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DC-DC high step-down split converters with low inductor current and low voltage stress – results for GaN-based design

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Abstract. This paper presents a concept of a DC-DC dual split buck converter with divided input voltage and a structure using two DC-DC switch-mode converters that supply the output capacitor in parallel. All components in the converter have reduced voltage stress, and the average current value of their inductors is reduced by about twofold compared to that of a buck converter. In the demonstrated implementation with GaN transistors, the converter achieved an efficiency higher than that of the buck converter, and its power range is also larger. The paper also proposes a solution where, at the output of the converter, there is a stack of capacitors with various connection configurations with the converter modules and load. Depending on the configuration, we achieve output current ripple cancelation, a further reduction by half in the average value of the inductor current, and a larger voltage control range. In addition, the converter operates with low voltage stress and has more than one output. An integral part of the converter in this configuration is an output balancing circuit. In the proposed implementation, this is a resonant switched-capacitor (SC) ladder converter based on low-voltage transistors of low resistance. This article contains results of experimental research on both types of converters based on GaN transistors with 400 kHz output current ripple and balancing circuit operation.

Keywords: high step-down converter; buck converter; GaN-based converter; DC power supply; switched-capacitor converter.

1. INTRODUCTION

In recent years, the applications of DC-DC power converters have continued to expand across diverse spheres, ranging from ultra-low power-driven Internet of Things (IoT) devices to large power-intensive fields such as electric vehicle (EV) systems, photovoltaic-based power generation systems, wind energy conversion systems, and energy storage systems. Many of these applications require DC-DC converters capable of handling wide input voltage variations while maintaining stable output regulation [1–3]. Moreover, many modern power electronic systems are required to manage extreme voltage conversion ratios with high efficiency and compact form factors. Conventional DC-DC converters, though simple and widely used, often become inefficient and impractical under such extreme step-up/step-down requirements. Their performance deteriorates due to ultra-low duty cycles ($D < 0.02$), resulting in poor control resolution and greater switching losses, while large current ripple and parasitic effects further reduce efficiency [4].

Hybrid DC-DC converters have emerged as a promising solution to address these challenges by combining switched-capacitor (SC) and switched-inductor (SL) techniques. These topologies leverage the high-power density characteristics of capacitive energy storage with the continuous energy transfer capabilities of inductive elements, thereby achieving high step-down conversion ratios with reduced voltage stress and lower conduction losses, as compared to the conventional approaches [5]. Recent development in hybrid DC-DC converter topologies has focused on multiple key challenges: high voltage conversion ratios with minimal component count, reducing voltage stress, minimizing passive component size, and improving transient response [6]. In [7], a hybrid SL/SC converter with a low inductor current, transistor peak stress, and improved efficiency (up to 98.5%) is proposed, while a bidirectional hybrid SC converter for a supercapacitor system is proposed in [8], which was further enhanced using GaN-based devices to reduce passive requirements and switching losses, and multi-stage configurations for extreme voltage reduction [9, 10]. In these converters, however, the cost rises greatly owing to the increased component count. A single-switch high step-up converter utilizing SL configuration with design simplicity is presented in [11]. A comparative performance analysis of regulated hybrid SC topologies is presented in [12], indicating im-

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proved performance of such topologies in various applications. A high-gain converter with low input current ripple and reduced voltage stress is discussed in [13], although it was experimentally demonstrated for low power. Another such converter, combining coupled inductors (CIs) with SCs, is presented in [14]. A more advanced version employing a three-winding CI converter with bipolar outputs and regenerative clamping, which uses leakage inductance to facilitate soft-switching, is proposed in [15]. The evolution toward quadratic and multi-stage converter designs has enabled even higher voltage conversion ratios. A single-switch high step-up quadratic converter with SC cells is proposed for DC microgrid application in [16]. In [17], a transformerless quadratic hybrid converter operating over a wide duty cycle range has been demonstrated. Another approach utilizes a modular-multilevel-converter-based hybrid SC design with bidirectional capability [18]. In [19], a fully soft-switching semi-interleaved converter is proposed, employing valley-fill capacitors. Similarly, an ultra-high step-up soft-switching converter that integrates interleaved operation with voltage multiplier stages is proposed in [20]. The converter described in [21] utilizes a series capacitor with CIs to facilitate zero-voltage switching (ZVS) across primary switches. In [22], a specialized converter topology incorporating voltage multiplier cells is introduced to achieve higher voltage gains at lower duty cycles. An integrated step-up/step-down converter implemented with SC circuits for battery-powered bioelectronics applications is presented in [23]. A remarkably helpful comprehensive survey of SC-based DC-DC converter topologies is described in [24], providing valuable insights into design characteristics, control strategies, and practical applications. Multi-stage approaches have further extended the capabilities of hybrid converters. For example, a multi-stage SL-SC high-gain converter integrating active-switch-capacitor (ASC) and active-passive-inductor-cell (APIC) components has demonstrated scalable voltage gain characteristics suitable for microgrid applications [25].

In [26], a transformerless quasi-resonant boost converter is presented that achieves a high degree of voltage gain and soft switching in the entire load power range. In [27] and [28], the results for bidirectional DC-DC systems with soft-switching operation are described, in which a coupled inductor and a flying capacitor are used. The use of SiC transistors allowed an efficiency of over 99%. A comprehensive study of power loss reduction in modified isolated and non-isolated boost DC-DC converters based on flyback, half-bridge, and push-pull topologies is presented in [29]. The use of a transformer allows for any conversion ratio to be set. At high switching frequencies, the transformer used can be compact; however, additional losses must be considered [30, 31].

Despite the aforementioned progress in hybrid DC-DC converters, there remains significant scope in conceptualizing novel topologies of DC-DC switch-mode converters and topologies with synergistic effects of combining SC and SL techniques, specific to the need for high step-down conversion.

In this paper, a novel approach to a switch-mode DC-DC converter is proposed which utilizes a split DC bus capacitor at the input stage to feed two anti-parallelly connected DC-DC converters, reducing voltage stress across transistors by operating each at half the input voltage. The use of such a converter concept (Split Buck Converter – SBC) also gives the following benefits compared to a synchronous buck converter:

- Higher efficiency
- A larger power range due to the division of the output current into two circuits and a lower current value of the inductors
- A higher ripple frequency allowing for a reduction in the capacitance of the input capacitors
- The input and output circuits with a shared direct connection, allowing us to create a system with a common input and output ground

This has been confirmed in tests of the system at a conversion ratio of 400-to-48 V, as for supplying a 48 V battery from high DC voltage.

A further modification of the proposed topology is a system in which the DC-DC converter, operating partly in two stages, has three series-connected outputs (HC3L). It can power a stack of three batteries or loads with any power asymmetry. The asymmetry is balanced by an output balancing circuit (BC) with switched capacitors. It is an extremely simple system that does not require a closed control loop. In such a case, the DC-DC converter operates with about a 50% reduction in inductor currents. Part of this concept is proposed in [7], where an analytical and simulation-based performance evaluation of the hybrid converter was performed. This paper extends the proposed concept with the following points:

- Introduction of new step-down converter topologies
- Proof of feasibility
- Experimental results that confirm the converter operation principle, parameters, and efficiency
- Results of bi-directional operation of the converter confirmed by experiments
- Input voltage balancing and basics of the control system
- Comparison to the state-of-the-art

The paper is structured as follows. In Section 2, the concept of a new DC-DC switch-mode converter is presented with its analytical model of efficiency. Section 3 discusses a hybrid converter that achieves a significant reduction in the average currents of the inductors. Section 4 presents the results of computer simulations of the proposed converters, and the design guidelines are summarized in Section 5. The experimental results are shown in Section 6.

2. HIGH STEP-DOWN DC-DC CONVERTER CONCEPT

2.1. Converter concept and basic properties

Figure 1 shows the concept of a DC-DC high step-down dual split buck converter (SBC). It is made up of two switch-mode converters connected to the capacitors of the input voltage divider.

The converter has been tested for voltage step-down operation. Compared to a DC-DC synchronous buck converter, it has the following advantages:

- Approximately 50% lower voltage stress on the components, which allows operation at a high frequency
- Larger output power range due to the two-way power supply of the output capacitor
- Higher ripple frequency

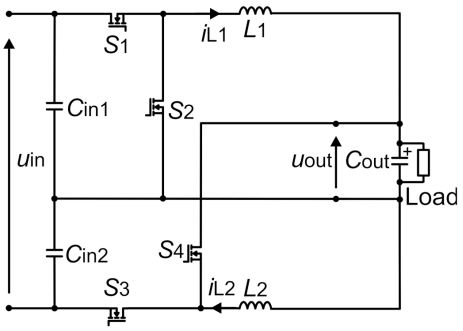


Fig. 1. Proposed DC-DC dual split buck converter (SBC)

Figure 2 shows the operating states of the SBC. The high-side (HSC) and low-side (LSC) converters operate independently of each other and have two operating states: the inductor energy increase state and the energy decrease state. The switching of these converters is synchronized, and the signals are phase-shifted (Fig. 3) to achieve an increase in the output current ripple frequency.

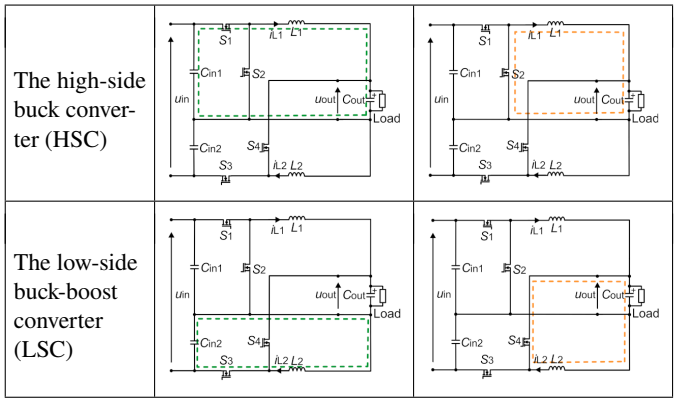


Fig. 2. States of operation of high- and low-side converters of SBC

The high-side converter (HSC) has a buck topology, while the low-side converter is a buck-boost. Assuming that both converters operate at an input voltage equal to $U_{\text{in}}/2$, their duty cycles are the following (D_1 – HSC and D_2 – LSC):

$$D_1 = \frac{U_{\text{out}}}{\frac{U_{\text{in}}}{2}} = 2\frac{U_{\text{out}}}{U_{\text{in}}}, \tag{1}$$

$$D_2 = \frac{U_{\text{out}}}{\frac{U_{\text{in}}}{2} + U_{\text{out}}} = \frac{D_1}{D_1 + 1}. \tag{2}$$

Equations (1) and (2) also indicate that the ratio of output to input voltage depends on the duty cycles of the control and can be adjusted continuously.

The voltage stress of the transistors is the following:

$$U_{\text{DS_}S1,S2} = \frac{U_{\text{in}}}{2}, \quad U_{\text{DS_}S3,S4} = \frac{U_{\text{in}}}{2} + U_{\text{out}}. \tag{3}$$

For the 400-to-48 V conversion, $U_{\text{DS_}S1,S2} = 200$ V and $U_{\text{DS_}S3,S4} = 248$ V.

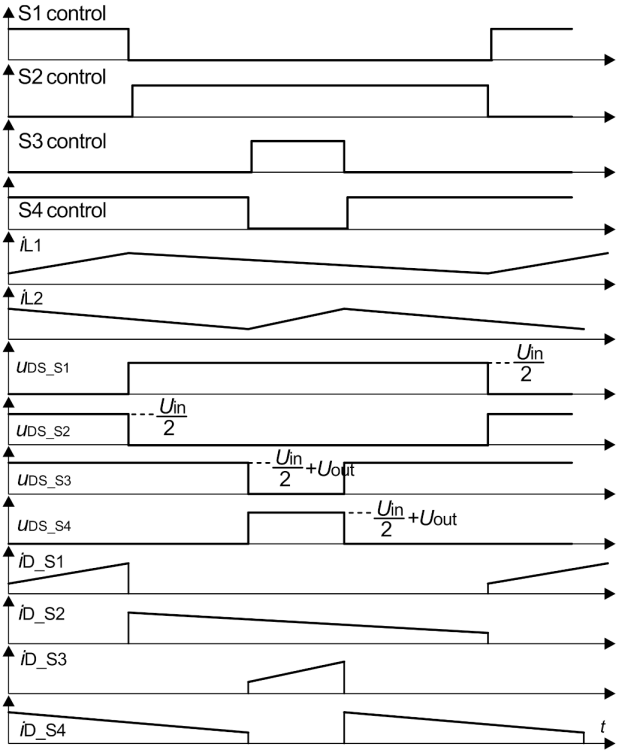


Fig. 3. Timing of control and operation of SBC (Fig. 1)

The current stress of the components is the following:

$$I_{L1\text{av}} = \frac{P_{\text{out}}}{2U_{\text{out}}}, \qquad I_{L2\text{av}} = \frac{I_{L1\text{av}}}{(1-D_2)}, \tag{4}$$

$$I_{\text{D_}S1} = I_{L1}\sqrt{D_1}, \qquad I_{\text{D_}S2} = I_{L1}\sqrt{1-D_1}, \tag{5}$$

$$I_{\text{D_}S3} = I_{L2}\sqrt{D_2}, \qquad I_{\text{D_}S4} = I_{L2}\sqrt{1-D_2}, \tag{6}$$

where

$$I_{L1} = \sqrt{I_{L1\text{av}}^2 + \frac{\Delta I_{L1}^2}{12}}, \quad I_{L2} = \sqrt{I_{L2\text{av}}^2 + \frac{\Delta I_{L2}^2}{12}} \tag{7}$$

are the RMS values of the inductor currents and

$$\Delta I_{L1} = \frac{U_{\text{out}}(1-D_1)}{L_1 f_s}, \quad \Delta I_{L2} = \frac{U_{\text{out}}(1-D_2)}{L_2 f_s} \tag{8}$$

are the peak-to-peak values of currents i_{L1} and i_{L2}.

2.2. Efficiency and comparison to the buck converter

It is assumed that $U_{\text{in}} = 400$ V, $U_{\text{in1}} = U_{\text{in2}} = U_{\text{in}}/2 = 200$ V, $U_{\text{out}} = 48$ V, and that both parts of the converter supply the same amount of power to the output ($P_{\text{buck}} = P_{\text{out}}/2$).

The efficiency of the converter is:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}, \tag{9}$$

where P_{loss} is the sum of losses in the converter.

Based on typical loss models for a switch-mode DC-DC converter, Fig. 4 shows the results of the efficiency calculation of the SBC for the 400-to-48 V conversion ratio, compared to those for a synchronous buck converter. The loss model is calculated using a set of equations collected in Table 1.

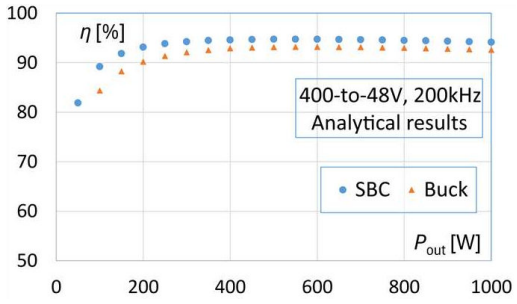


Fig. 4. Efficiency of the proposed SBC (Fig. 1) and a synchronous buck converter – analytical results. Conversion ratio: 400V/48V

Table 1
Losses model of SBC

Origin of losses	Formula
Resistive loss in inductors and S_1–S_4 branches (R_{Sn} is the sum of $R_{DS(on)}$ and parasitic resistances in the branch)	Inductors: $P_{L1cond} = R_{L1} I_{L1}^2$, $P_{L2cond} = R_{L2} I_{L2}^2$, S_1: $P_{S1cond} = R_{S1} I_{D_S1}^2$, S_2: $P_{S2cond} = R_{S2} I_{D_S2}^2$, S_3: $P_{S3cond} = R_{S3} I_{D_S3}^2$, S_4: $P_{S4cond} = R_{S4} I_{D_S4}^2$, where the currents are given by equations (5)–(7).
Overlapping during transistor switching	$P_{swS1(3)} = 0.5 f_S U_{DS_S1(3)} \left(I_{L1(2)av} - \Delta I_{L1(2)}/2\right)(t_{cr} + t_{vf}) + 0.5 f_S U_{DS_S1(3)} \left(I_{L1(2)av} + \Delta I_{L1(2)}/2\right)(t_{cf} + t_{vr})$
Capacitive loss (C_{oSn} is the sum of C_{ossn} and parasitic capacitances)	$P_{oS1} = 0.5 f_S C_{oS1} U_{DS_S1}^2$ $P_{oS3} = 0.5 f_S C_{oS3} U_{DS_S3}^2$
ESR	$P_{Cin1(2)} = \mathrm{ESR}_{C1(2)} I_{L1(2)av}^2 (1 - D_{1(2)}) D_{1(2)}$ $P_{Cout} = \mathrm{ESR}_{Cout} \left[\Delta I_{L1}^2/12 + I_{L2av}^2 (1 - D_2)\right]$
Dead-time	$P_{dt1(2)} = f_S t_d \left[U_{SD} I_{L1(2)av} + R_{DS(on)} I_{L1(2)max}^2\right]$
Core	Customer calculator and estimation for 74437529203151 – based on [32]
Assumed parameters: $R_{DS(on)S1S3} = 55$ mΩ, $R_{DS(on)S2S4} = 35$ mΩ at 25°C, $R_{stray} = 0.5$ mΩ in each branch, $C_{oss(er)S1(3)} = 65$ pF, $C_{oss(er)S2(4)} = 150$ pF, inductor $R_{DC} = 15$ mΩ, $\mathrm{ESR}_{Cout} = 1$ mΩ, $\mathrm{ESR}_{Cin} = 1$ mΩ, $P_{core} = 0.35$ W, $C_{parasitic} = 500$ pF, transistor temperature range: $T_j = 25$–100°C, $R_{DS(on)}$ vs. T: based on transistor datasheet, $R_{PCB/windings}$ vs. temperature: 0.39% per °C (assumed $\Delta T = 25$–75°C), gate driver losses $P_g = Q_g U_{GS} f_S$ (not included in measurement results); t_{cf}, t_{cr}, t_{vf}, t_{vr}, denote current and voltage fall and rise time during switching of transistors. C_{oss} losses are also increased by losses in transistors S_2 and S_4 at light load and resistive losses associated with the output capacitances of the transistors charging. $U_{SD} = 2.4$ V (Source-Drain Reverse Voltage); $t_d = 20$ ns.	

The proposed SBC converter has higher efficiency than a synchronous buck converter, for two main reasons:

- Lowering the voltage across the transistors at the turn-ons (equation (3)), which results in a reduction in P_{oss}:

$$P_{oss(SBC)} = f_S \frac{1}{8} C_{oss} U_{in}^2 + f_S \frac{1}{2} C_{oss} \left(\frac{U_{in}}{2} + U_{out}\right)^2, \qquad (10)$$

$$P_{oss(buck)} = f_S \frac{1}{2} C_{oss} U_{in}^2. \qquad (11)$$

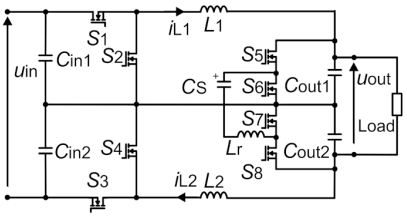
- The output current is divided into two branches; this decreases the RMS value of the currents, and the result is a reduction in conduction losses I^2R.

3. IMPROVEMENT OF PARAMETERS IN HYBRID CONVERTERS

In the case of supplying a stack of more than one battery or load, an integral part of the converter can be an active balancing circuit (BC). Such converters are called here "hybrid converters". This circuit, using switched capacitors, has a low-complexity design and control, operates in an open loop, and leads to equalization of voltages across the output capacitors connected in series. In addition, the BC works with voltage stress resulting from the output voltage, allowing the use of transistors with exceptionally low resistance. A beneficial aspect of the pseudo-two-stage transformation with an active voltage balancing circuit BC on the output capacitor stack is a reduction in the average value of the inductor current and continuous output capacitor current.

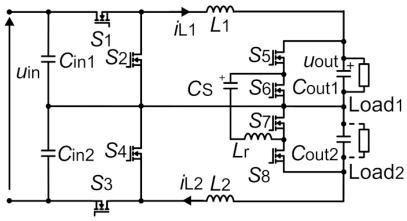
3.1. Hybrid converters with continuous output capacitor current

Figure 5 shows the concept of split converters with a continuous output capacitor current. In each case, u_{out} is equal to 48 V. The high- and low-side buck converters supply separate output capacitors with voltages of the same polarity. The balancing circuit (BC) in the switched-capacitor (SC) ladder topology, like the one presented in [33], equalizes the voltages on the output capacitors. If only one capacitor is loaded, the BC works at 50% of P_{out}, but if their load is the same, the BC power equals zero.



$U_{in} = 400$ V
$U_{Cout1} = 24$ V
$U_{Cout2} = 24$ V
$U_{out} = 48$ V
$D_{1,2} = 2U_{Cout1,2}/U_{in}$
$U_{DS_S1-S4} = 200$ V
$I_{L1,2av} = P_{out}/U_{Cout1} = (P_{out}/24)$ A

(a) Hybrid converter for a single load (HC1L), low voltage stress, and low load of balancing circuit BC



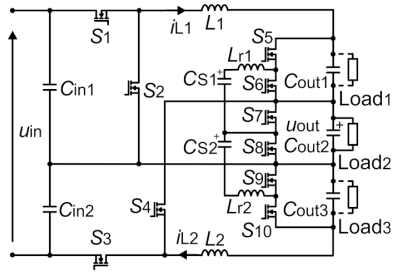
$U_{in} = 400$ V
$U_{Cout1} = 48$ V
$U_{Cout2} = 48$ V
$U_{out} = 48$ V
$D_{1,2} = 2U_{Cout1,2}/U_{in}$
$U_{DS_S1-S4} = 200$ V
$I_{L1,2av} = (P_{out}/48)$ A

(b) Hybrid converter for two loads (HC2L), low voltage stress, decreased inductor current, and nonzero load of balancing circuit BC in case of load asymmetry

Fig. 5. Proposed hybrid converters with continuous output capacitor current

3.2. Hybrid converter with three outputs

The converters shown in Fig. 5 can be further modified to achieve a significant reduction in the average current of the inductors, partial power conversion in the second stage, and operation with an increased voltage range. The converter presented in Fig. 6 (hereafter called HC3L – hybrid converter with three outputs), consisting of three parts: high-side switch-mode buck converter (HSC2), low-side switch-mode buck-boost converter (LSC2), and balancing circuit (BC), contains three output capacitors in a stack.



$U_{\text{in}} = 400$ V
$U_{C\text{out1}} = 48$ V
$U_{C\text{out2}} = 48$ V
$U_{C\text{out3}} = 48$ V
$U_{\text{out}} = 48$ V
$D_1 = 2U_{\text{out}}/(U_{\text{in}}/2)$
$D_2 = 2U_{\text{out}}/(U_{\text{in}}/2+U_{\text{out}})$
$U_{\text{DS_}S1,S2} = 200$ V
$U_{\text{DS_}S3,S4} = 248$ V
$I_{L1,2\text{av}} = (P_{\text{out}}/96)$ A

Fig. 6. Proposed hybrid converter (HC3L) with low continuous inductor currents

The output currents of inductors L_1 and L_2 are reduced by about 50% compared to those of the SBC (Fig. 1). In the HC3L, the switch-mode input converters charge the output capacitor C_{out2}, as well as capacitor C_{out1} (charged by the high-side converter HSC2) and C_{out3} (charged by the low-side converter LSC2). Capacitor C_{out2} is charged by both converters with twice the power delivered to capacitors C_{out1} and C_{out3}. The system works as a pseudo-two-stage converter, and the output balancing circuit BC (SC ladder composed of two switched capacitors) operates with 50% of output power P_{out}.

$$u_{\text{out_HSC2}} = u_{C\text{out1}} + u_{C\text{out2}}, \quad u_{\text{out_LSC2}} = u_{C\text{out2}} + u_{C\text{out3}}. \tag{12}$$

Assuming that both HSC2 and LSC2 generate the same voltage, their output voltage reaches the upper limit at $u_{C\text{out}n} = U_{\text{in}}/4$:

$$u_{\text{out_HSC2}} = u_{\text{out_LSC2}} = \frac{U_{\text{in}}}{2}. \tag{13}$$

The total output voltage (across the whole output stack in Fig. 6) is

$$U_{\text{outmax}} = 3u_{C\text{out}n} = \frac{3}{4}U_{\text{in}}. \tag{14}$$

Assuming that $U_{\text{out}} = 48$ V and $U_{\text{in max}} = 400$ V, $U_{\text{DS_}S3,S4\,\text{max}} = 248$ V. The minimum input voltage value for the SBC (Fig. 1) is $U_{\text{in}-\text{min SBC}} = 96$ V, and for the HC3L, $U_{\text{in}-\text{min HC3L}} = 72$ V.

The operation states of the HSC2, LSC2, and the balancing converter (BC) in this topology are shown in Figs. 7 and 8. The BC equalizes the output voltages of the output capacitors in all load cases. It is assumed that the main output of the system is capacitor C_{out2} because it is charged by both the switch-mode converters HSC2 and LSC2. Two border cases of BC load can be distinguished, which will be investigated.

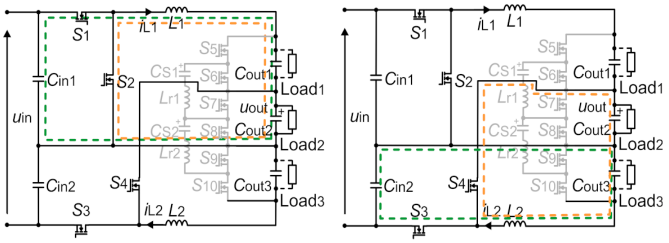


Fig. 7. States of operation of switch-mode converters in HC3L (Fig. 6)

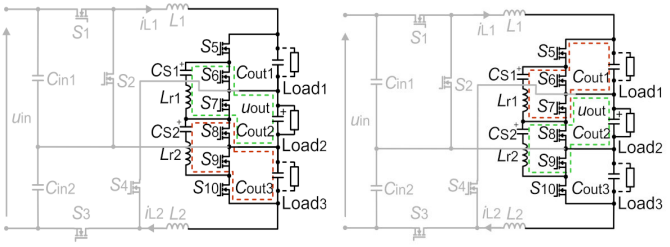


Fig. 8. States of operation of balancing circuit (BC) in HC3L

The BC operates at maximum power if

$$P_{\text{Load1}} = P_{\text{Load3}} = 0, \quad P_{\text{out}} = P_{\text{Load2}}, \quad P_{\text{balancer}} = P_{\text{out}}/2. \tag{15}$$

The BC operates at zero power if

$$P_{\text{Load1}} = P_{\text{Load3}} = \frac{P_{\text{out}}}{4}, \quad P_{\text{Load2}} = \frac{P_{\text{out}}}{2}, \quad P_{\text{balancer}} = 0. \tag{16}$$

It should be mentioned that there are also other cases of load asymmetry.

The voltage stress of the transistors in the BC is

$$U_{\text{DS_}S5-S10} = U_{\text{out}}. \tag{17}$$

The control in the hybrid systems is analogous to that in the SBC (Fig. 1). Only the conversion ratios of the switch-mode converters should be considered. The BC is controlled with the use of a half-period duty cycle and operates in an open control loop. The timing diagram for the HC3L (Fig. 6) is shown in Fig. 9. The efficiency of the switch-mode part in this converter can be calculated in a similar way to that of the SBC (Fig. 1). An important difference is that the average current of the inductors is lower than that in the SBC.

In the hybrid converter, the balancing circuit (BC) can generate power losses. These are conduction losses in transistors and LC elements of the resonant circuit, losses in the core of resonant inductors, and C_{oss} losses. These losses can be determined by assuming that the BC operates with a sinusoidal current waveform and zero current switching (ZCS) occurs. With the voltage stress of transistors S_5-S_{10} at the output voltage level (in the tested case $U_{\text{DS_}S5-S10} = 0.12U_{\text{in}}$), the C_{oss} losses are small, and the choice of ZCS control is advantageous. The total value of power losses in the output balancing circuit (BC) is the sum of conduction loss ($P_{S\text{cond}}$) and $P_{C\text{oss}}$ loss in transistors S_{5-10}, loss in resistances ($P_{L\text{cond}}$) and cores (P_{core}) of the inductors,

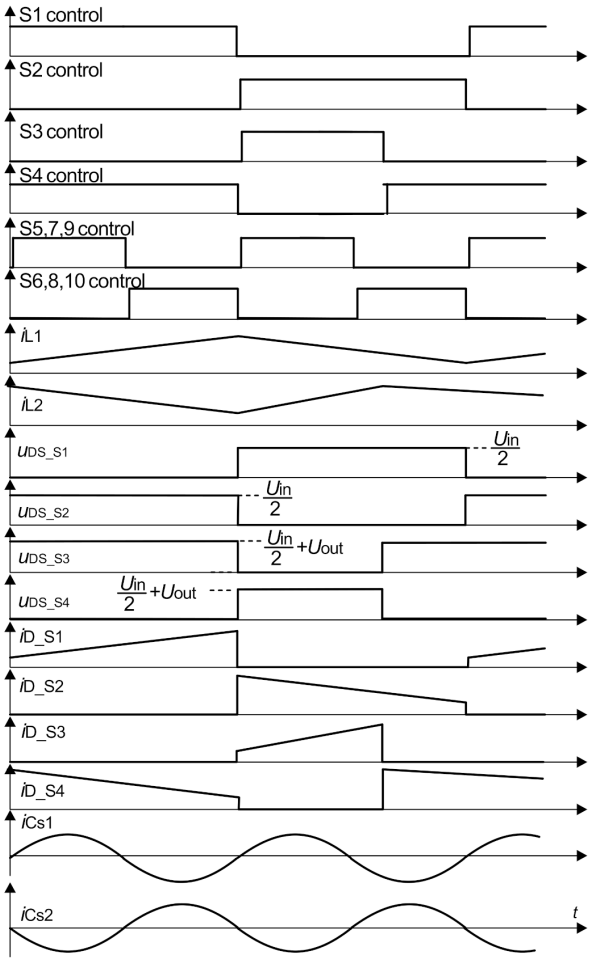


Fig. 9. Timing of control and operation of HC3L (Fig. 6)

and parasitic losses in the PCB (P_{PCB}) and ESRs (P_{ESR}) of the capacitors:

$$P_{\mathrm{bal_loss}} = P_{S\mathrm{cond}} + P_{C\mathrm{oss}} + P_{L\mathrm{cond}} + P_{\mathrm{core}} + P_{\mathrm{PCB}} + P_{\mathrm{ESR}}\,. \quad (18)$$

Figure 10 shows the analytical result of the efficiency calculation of the HC3L (including the BC) compared to that of the SBC in Fig. 1. In the case presented, the hybrid system HC3L operates with a single load attached to the center capacitor (C_{out2}), and this is the heaviest load condition in relation to the output power.

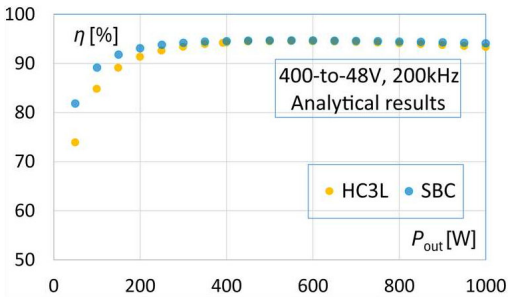


Fig. 10. Efficiency of hybrid converter HC3L with a single load (Fig. 6, $P_{\mathrm{Load2}} = P_{\mathrm{load}}$, $P_{\mathrm{Load1}} = P_{\mathrm{Load3}} = 0$ W) and SBC (Fig. 1) – analytical results. Conversion ratio: 400V/48V

Under load on other output capacitors, the power of the BC decreases and can reach zero watts. From the results presented in Fig. 10, it is seen that the hybrid system slightly reduces the efficiency of the converter.

The general control structure for the HC3L system or SBC can be very similar to typical switching converter control systems. Figure 11 shows the concept of a system with a voltage regulator. The atypical parts here are the signal generator module for the balancing circuit BC (switching with a 50% duty cycle) and the calculation of the duty cycle for the buck-boost system, according to equation (2).

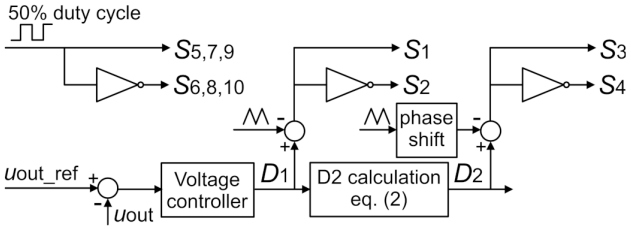


Fig. 11. Control system of HC3L and SBC

4. SIMULATION RESULTS

The simulation test parameters are summarized in Table 2. The simulation was carried out for an output voltage of 48 V, as this is one of the typical voltage values of batteries.

Table 2
Parameters for waveform simulations

Parameter	Description and value
Simulation method and transistor models	MATLAB/Simulink/Simscape Electrical
Input voltage	$U_{\mathrm{in}} = 400$ V
Output voltage (across capacitor C_{out2})	$U_{\mathrm{out}} = 48$ V
Inductors in switch-mode converters	$L_1 = L_2 = 150$ µH
Inductors in SC circuits (BC)	$L_{\mathrm{r1}} = L_{\mathrm{r2}} = 1$ µH
Capacitors in SC circuits (BC)	$C_{\mathrm{S1}} = C_{\mathrm{S2}} = 168$ nF
Switching frequency of a single switch	$f_{\mathrm{S}} = 200$ kHz – switch mode $f_{\mathrm{b}} = 400$ kHz – BC
Dead time	$t_{\mathrm{d}} = 20$ ns

4.1. Operation of the SBC

An advantage of the proposed SBC (Fig. 1) is the reduction in the voltage stress of the components and in the current of the inductors compared to those in a synchronous buck converter. The current of the components is also more symmetric, and the current and output voltage ripples are reduced.

Figure 12 shows the waveforms in steady state. From these waveforms, it can be seen that the voltage stress of the transistors

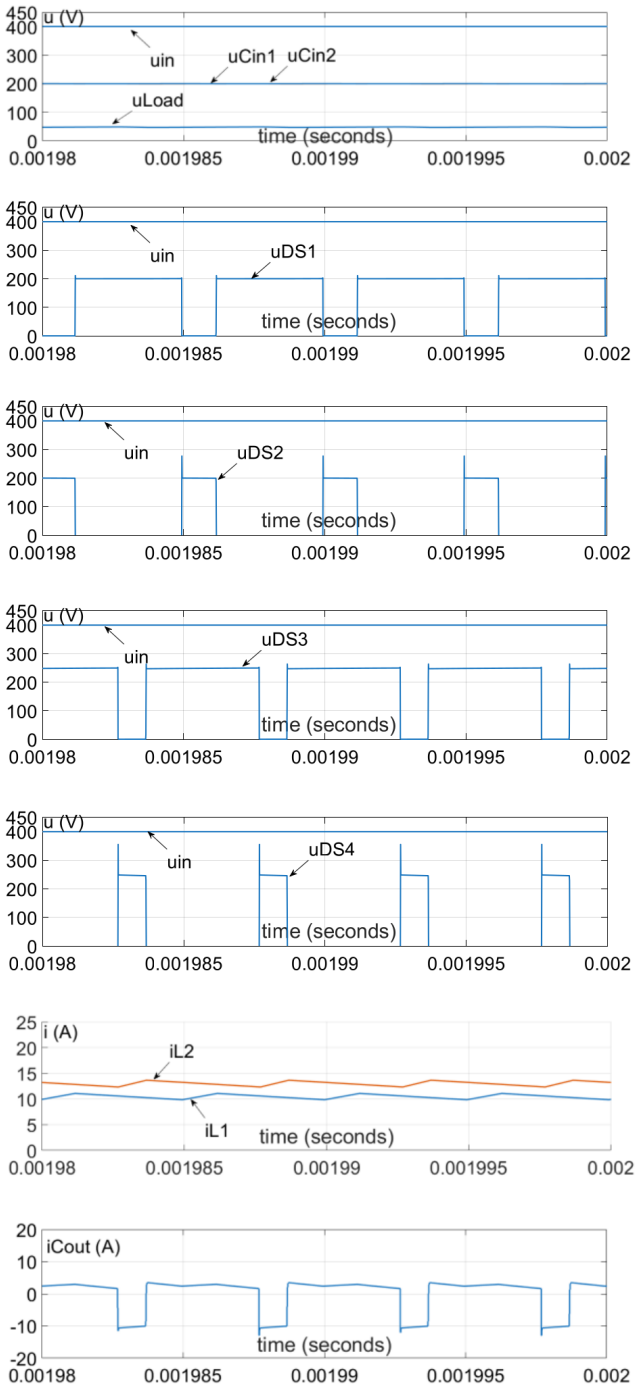


Fig. 12. Steady-state waveforms in SBC: voltage across input capacitors (u_{Cin1}, u_{Cin2}), output voltage ($u_{out} = u_{Load}$), voltages across transistors, inductor currents, and current of the output capacitor. $U_{in} = 400$ V, $P_{load} = 1000$ W, $f_S = 200$ kHz

of the up-side circuit (HSC) is $U_{DS} = U_{in}/2$ and that of the inductor $U_{L1} = (-U_{out}$ to $U_{in}/2 - U_{out})$. For the low-side buck-boost converter (LSC), $U_{DS} = U_{in}/2 + U_{out}$, $U_{L2} = (-U_{out}$ to $U_{in}/2)$.

The average value of the inductor currents at $P_{out} = 1000$ W is approximately $I_{L1av} = 10.5$ A and $I_{L2av} = 13$ A. The ripple frequency in the output voltage is 200 kHz.

Active balancing of input voltages is not required in the system, as they remain at the correct level while maintaining the appropriate duty cycles for both converters according to the typical dependencies (1) and (2).

4.2. Operation of the hybrid converters

The concept of charging two output capacitors, as shown in Figs. 5a and 5b, requires the use of a circuit that equalizes the voltage on these capacitors. This converter with a load attached to two output capacitors becomes close to a ripple-free one, while the active balancing circuit (BC) operates with very little power and acts as protection. This system eliminates the disadvantage of the SBC (Fig. 1), which is the output current ripple caused by the low-side buck-boost converter (LSC). The voltage stress of the transistors remains close to $U_{in}/2$. However, the disadvantage of this solution is a high average current in the inductors, because the high- and low-side converters work with a conversion ratio of 200V/24V. This is demonstrated in the waveforms shown in Fig. 13.

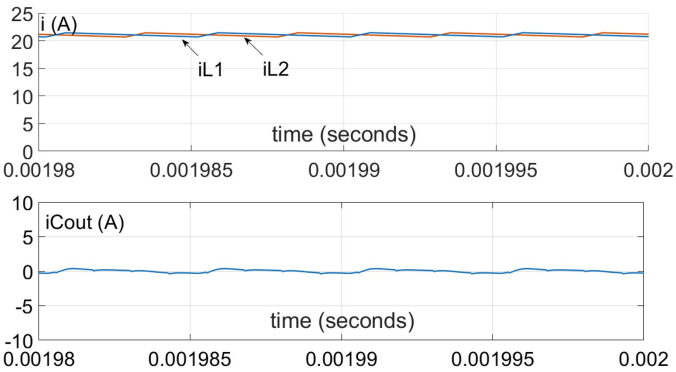


Fig. 13. Inductor currents and output capacitor current in the hybrid converter HC1L with two output capacitors and load connected to two output capacitors (Fig. 5a)

When adding a load to one of the capacitors, the high- and low-side circuits work with a conversion ratio of 200V/48V, which allows one to work with half the current of the inductors (Fig. 5b). The energy of one of the capacitors is transferred to the load through the balancing circuit (BC). The current waveform of the resonant inductor and the current in the output capacitor are shown in Fig. 14. The converter from Fig. 5b is a remarkably advantageous solution for connecting two 48 V loads, e.g., two batteries connected in series. In this case, it works with a small current in the inductors in the switch-mode part and without loading the balancing circuit (BC). The current of the switch-mode converter inductors can be further significantly reduced by modifying the output circuit of the converter in such a way that the high- and low-side circuits operate at the 200/96 conversion ratio. This is possible in the hybrid system HC3L shown in Fig. 6.

The high- and low-side circuits supply two output capacitors each, and the active balancing circuit (BC) operating in the second conversion stage equalizes the voltages on the output capacitors. This system is also very advantageous for powering three consumers – for example, a stack of three batteries –

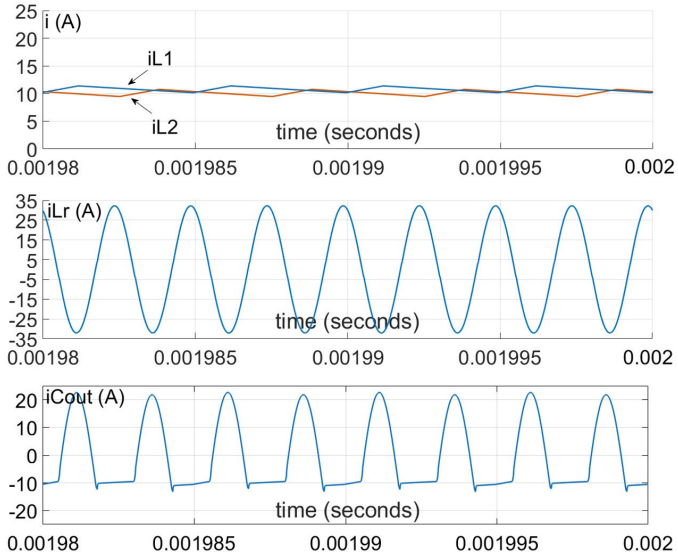


Fig. 14. Inductor current and output capacitor current in the hybrid converter HC2L with load connected to one output capacitor (Fig. 5b). $P_{\text{Load1}} = 1000$ W, $P_{\text{Load2}} = 0$ W

because in that case the inductor current is low and the BC power is zero. However, even when powering a single load, this solution is much more beneficial than the hybrid HC2L system with two output capacitors (Fig. 5b, Fig. 16).

Figure 15 shows the waveforms of the input voltage and output voltages in such a system. The values of the input voltages are analogous to those in the basic system (Fig. 1), so the voltage stress of the low-side system elements is 248 V.

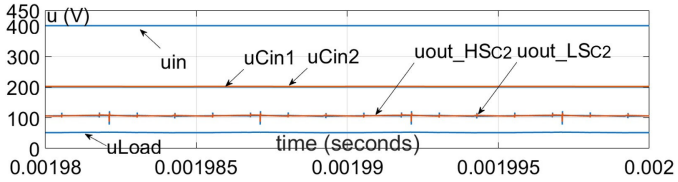


Fig. 15. Steady-state waveforms in hybrid converter HC3L (Fig. 6): input voltage, voltage across input capacitors ($u_{C\text{in}1}$, $u_{C\text{in}2}$), output voltage (u_{Load}), output voltage of switch-mode converters HSC2 ($u_{\text{out_HSC2}}$) and HSL2 ($u_{\text{out_LSC2}}$). $U_{\text{in}} = 400$ V, $P_{\text{load}} = 1000$ W, $f_{\text{S}} = 200$ kHz

Figure 16 presents a comparison of the steady-state inductor current waveforms in the hybrid converter with three (Fig. 6) and two output capacitors (Fig. 5b). In both cases, the circuits operate with a load attached to a single capacitor. This is the most load-bearing operating case for the balancing circuit (BC). The waveforms in the system with two output capacitors are presented using a dashed line. From the waveforms presented in Fig. 16, it can be seen that the hybrid converter with three output capacitors has a significantly reduced average value of the inductor current, the current of the BC, and the current ripple in the output capacitor. In addition, the inductor currents in the hybrid system HC3L with three output capacitors (Fig. 6) have a mean value half that of the SBC converter.

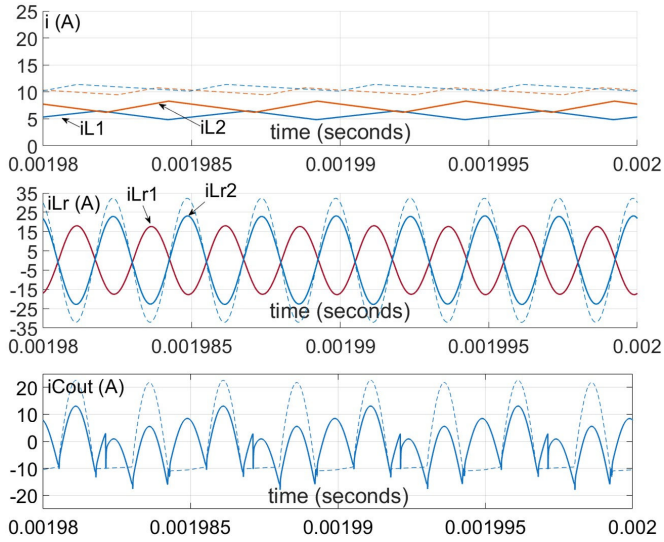


Fig. 16. Comparison of waveforms in the hybrid converters: HC3L with three output capacitors (Fig. 6) at $P_{\text{Load1}} = 0$ W, $P_{\text{Load2}} = 1000$ W, $P_{\text{Load3}} = 0$ W (solid line), and HC2L with two output capacitors (Fig. 5b) at $P_{\text{Load1}} = 1000$ W, $P_{\text{Load2}} = 0$ W (dotted line)

Both switch-mode parts of the SBC and HC3L have extremely favorable voltage stress conditions because they operate at the voltage across the input divider capacitors. The voltage stress of the transistors is listed in Table 3.

Table 3
Voltage stress across transistors (p.u is related to input voltage U_{in}) for SBC and HC3L

Device	S_1, S_2	S_3, S_4	S_5–S_{10}
Voltage p.u.	0.5	$0.5 + \frac{U_{\text{out}}}{U_{\text{in}}} = 0.62$	0.12

Figure 17 presents the operation of the SBC with a closed voltage control loop in transient states, such as the input voltage change between 400 V and 350 V and the load change between 450 W and 500 W. The converter exhibits stable operation and output voltage control ability. The control system allows the output capacitor to be charged at the start of the converter.

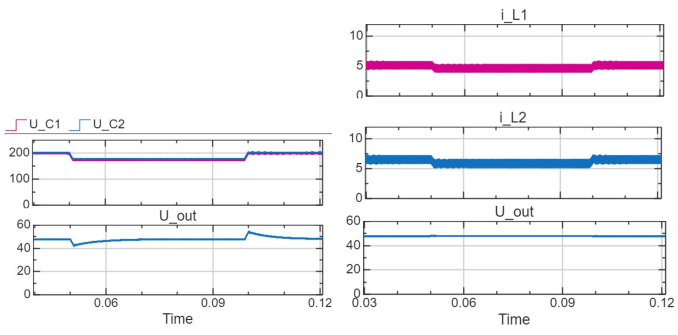


Fig. 17. SBC control system operation using PI-type voltage controller

DC-link input capacitors can usually be charged using a series resistor, and their balance when the converter does not operate can be maintained by a low-power resistive divider.

5. DESIGN GUIDELINES

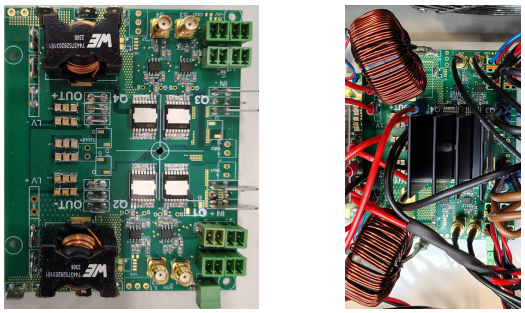
The guidelines for the design are very clear since they are based on the relevant assumptions, voltage stress estimation, and power losses calculated in the previous sections:

- Selection of the LC elements of the switch-mode parts: based on the current ripple, voltage limit, and the switching frequency.
- Selection of switch-mode circuit transistors: It considers reduced voltage stress in the topology with a voltage divider; $R_{DS(on)}$ results from the conduction-loss limit; transistor type and switching losses determine the frequency limit.
- Breakdown voltage of BC transistors: It results from the voltage stress, which is $U_{DS_S5-S10\,max} < 2U_{out}$.
- The capacitance of the BC capacitors results from the maximum power at which this circuit operates; the inductance of the BC inductor ensures an oscillating current waveform and results from C_{Sn} and the switching frequency: $L_{rn} = 1/(4\pi^2 f_S^2 C_{Sn})$.

6. EXPERIMENTAL RESULTS

6.1. Split buck converter (SBC)

Figure 18 shows the laboratory system for testing the proposed SBC (Fig. 1). Its parameters are presented in Table 4.



(a) (b)

Fig. 18. Experimental SBC (Fig. 1); (a) PCB board with elements, (b) converter tested with the second variant of inductors implemented

Figures 19 and 20 show the waveforms of the SBC (Fig. 1) with the output voltage set to 48 V (Fig. 19) or 120 V (Fig. 20) according to equations (1) and (2). For equal values of the input divider capacitor voltage ($U_{in1} = U_{in2}$), the voltage stresses across the transistors are about half the input voltage: $U_{DS_S1-S2} = U_{in}/2$ and $U_{DS_S3-S4} = (U_{in}/2 + U_{out})$.

The waveforms shown in Fig. 19 confirm the principle of operation of the system and the simulation results. The total input voltage is $U_{in} = 400$ V; the voltages on the input divider are maintained at the correct level equal to half of the input

Table 4
Parameters of the experimental model of SBC

Parameter	Description and value
Input voltage	$U_{in} = 400$ V
Output voltage (U_{out})	$U_{out} = 48$ V, 72 V, 120 V
Inductors*	$L = 150$ µH, $I_{SAT,30\%} = 8$ A (74437529203151 device) $L = 150$ µH, $I_{rated} = 15$ A (NAC-15-0151 device)
Transistors	S_1, S_3: IGLT65R055D2, $U_{DS} = 650$ V, $I_D = 31$ A, $R_{DS(on)} = 55$ mΩ (typ. value at 25°C), $C_{oss} = 57$ pF S_2, S_4: IGLT65R025D2, $U_{DS} = 650$ V, $I_D = 67$ A $R_{DS(on)} = 25$ mΩ (typ. value at 25°C), $C_{oss} = 130$ pF
Switching frequency of a single transistor	$f_S = 200$ kHz
Dead time	$t_d = 20$ ns

* The design variant with inductor 74437529203151 (Fig. 18a) was used in preliminary tests. The second design variant with inductor NAC-15-0151 was used in the experimental tests finally demonstrated (Figs. 28–32) to produce a power up to $P_{out} = 1000$ W.

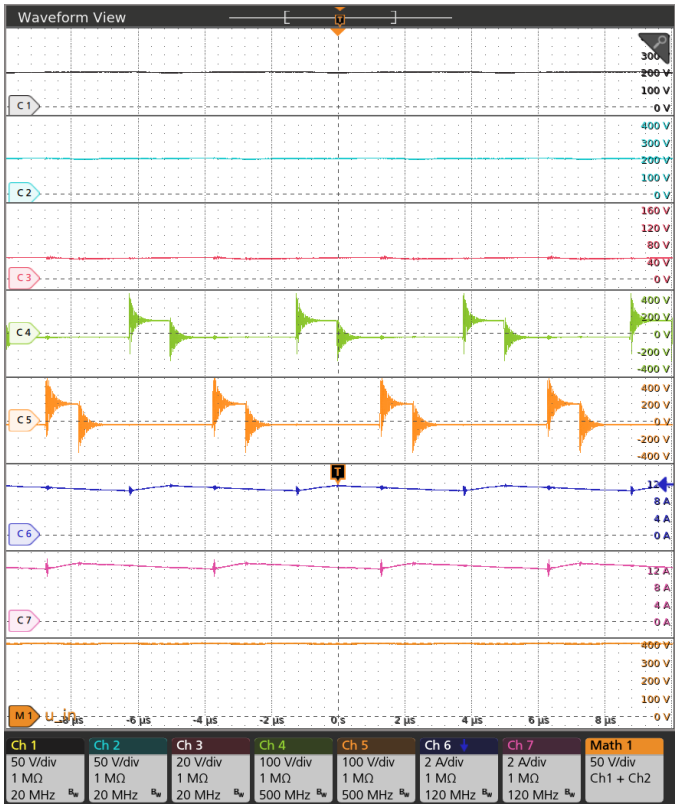


Fig. 19. Steady-state waveforms of SBC (Fig. 1) at 400V/48V, f_S = 200 kHz and $P_{out} = 1000$ W; C1: u_{C1in}, C2: u_{C2in}, C3: u_{out}, C4: u_{L1}, C5: u_{L2}, C6: i_{L1}, C7: i_{L2}, M1: u_{in}

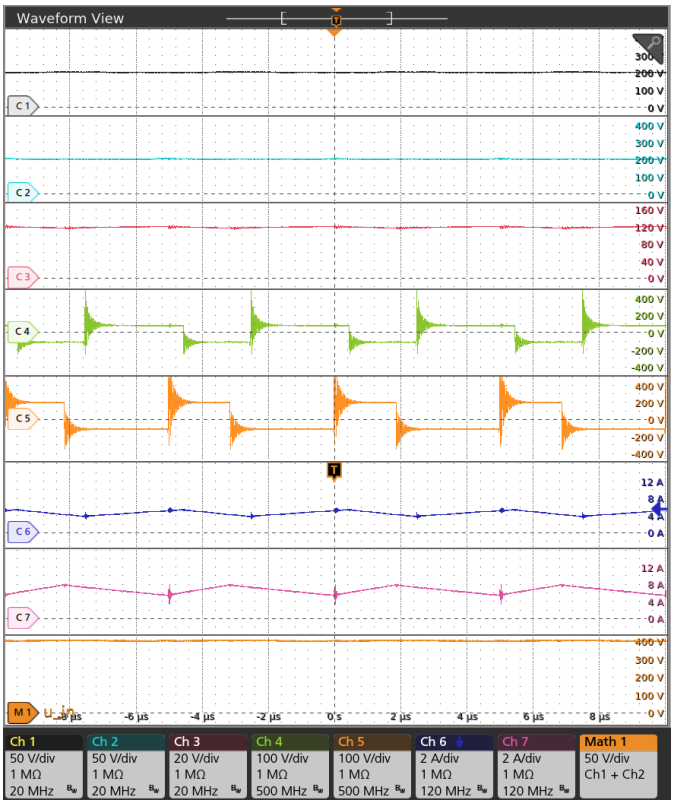


Fig. 20. Steady-state waveforms of SBC (Fig. 1) at 400V/120V; f_S = 200 kHz and P_{out} = 1000 W; C1: u_{C1in}, C2: u_{C2in}, C3: u_{out}, C4: u_{L1}, C5: u_{L2}, C6: i_{L1}, C7: i_{L2}, M1: u_{in}

voltage, $U_{C1in} = U_{C2in} = 200$ V; the inductor voltages are $U_{L1} = (-U_{out}$ to $U_{in}/2 - U_{out})$, $U_{L2} = (-U_{out}$ to $U_{in}/2)$, and the variable components of the inductor currents are in counterphase. The average value of the inductor currents is approximately twice as small as that which would occur in a buck converter ($I_{Lbuckav}$ = 1000 W/48 V = 20.8 A).

Compared to the DC-DC buck converter, the proposed SBC converter (Fig. 1) has a higher efficiency for the transistor switching frequency of 200 kHz. This converter also has a larger power range due to the lower average value of the inductor current and ripple. Figure 21 compares the efficiency of a synchronous DC-DC buck converter and the presented SBC converter (Fig. 1). To measure the efficiency of the synchronous buck converter, a fragment of the SBC converter with elements S_1, S_2, L_1, and

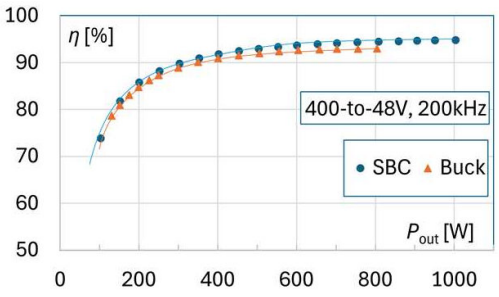


Fig. 21. Experimental efficiency measurement results of SBC (Fig. 1) and synchronous buck converter. Conversion ratio: 400V/48V

C_{in1} was used, and the input voltage was attached to capacitor C_{in1}. These relationships are similar to those obtained analytically. The discrepancies result mainly from the estimation of parasitic, capacitive, and resistive parameters.

Figure 22 shows the efficiency characteristics of the SBC that operates at other conversion ratios that may occur when working with batteries. The increase in the output voltage results in an increase in the voltage stress of the LSC and in C_{oss} loss. Therefore, this converter is designed to operate at a high conversion ratio.

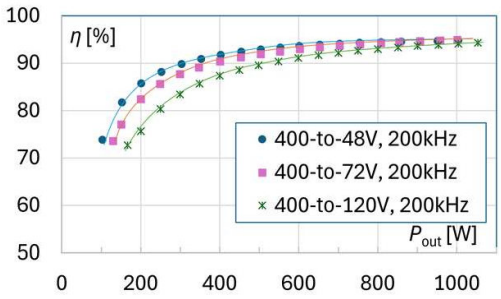


Fig. 22. Experimental efficiency measurement results of SBC (Fig. 1) for various conversion ratio values

Figure 23 shows the experimental results of the operation of the SBC converter during a load transient. The converter operates without input voltage balance control, and the load change does not cause an imbalance. The SBC (Fig. 1) can operate in boost mode when supplied from the output side. Figure 24 shows the waveforms in this case of operation, and Fig. 25 shows the efficiency compared to that of the classic boost converter. The proposed SBC exhibits higher efficiency in the entire tested output power range (up to 1000 W).

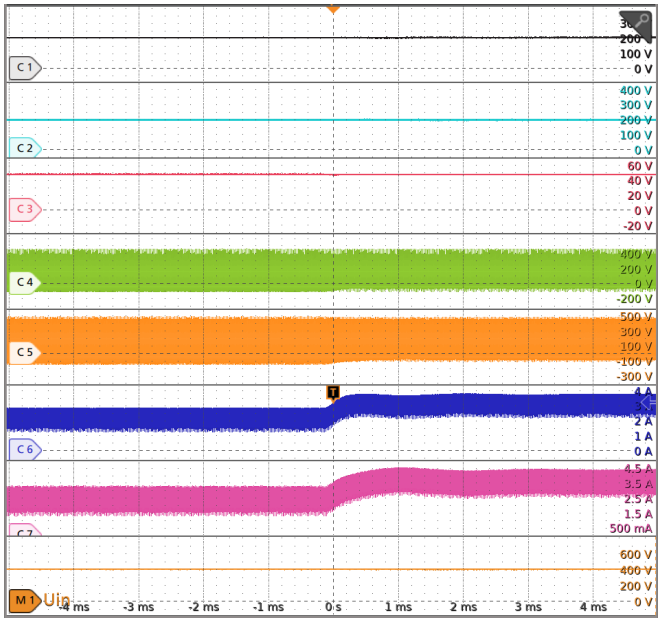


Fig. 23. Operation of SBC (Fig. 1) during load transient. P_{outmin} = 200 W, P_{outmax} = 300 W. C1: u_{C1in}, C2: u_{C2in}, C3: u_{out}, C4: u_{L1}, C5: u_{L2}, C6: i_{L1}, C7: i_{L2}, M1: u_{in}. Conversion ratio: 400V/48V

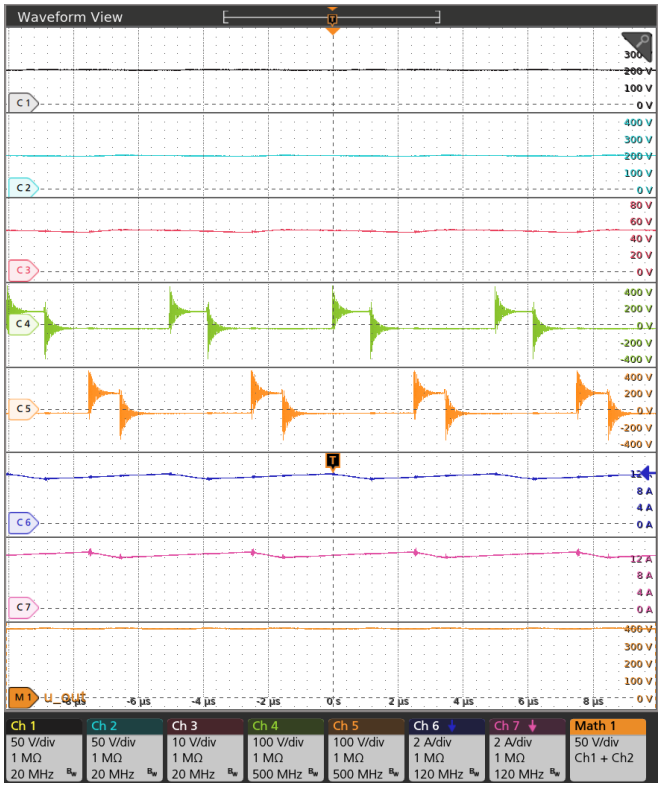


Fig. 24. Steady-state waveforms of SBC at boost mode operation at 48V/400V, f_S = 200 kHz and P_{out} = 1000 W. C1: u_{Cin1}, C2: u_{Cin2}, C3: input voltage, C4: u_{L1}, C5: u_{L2}, C6: i_{L1}, C7: i_{L2}, M1: output voltage

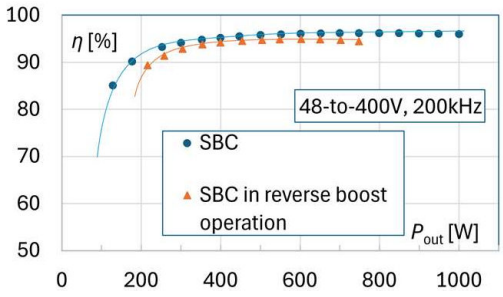


Fig. 25. Experimental efficiency measurement results of SBC (Fig. 1) at boost mode operation. Conversion ratio: 48V/400V

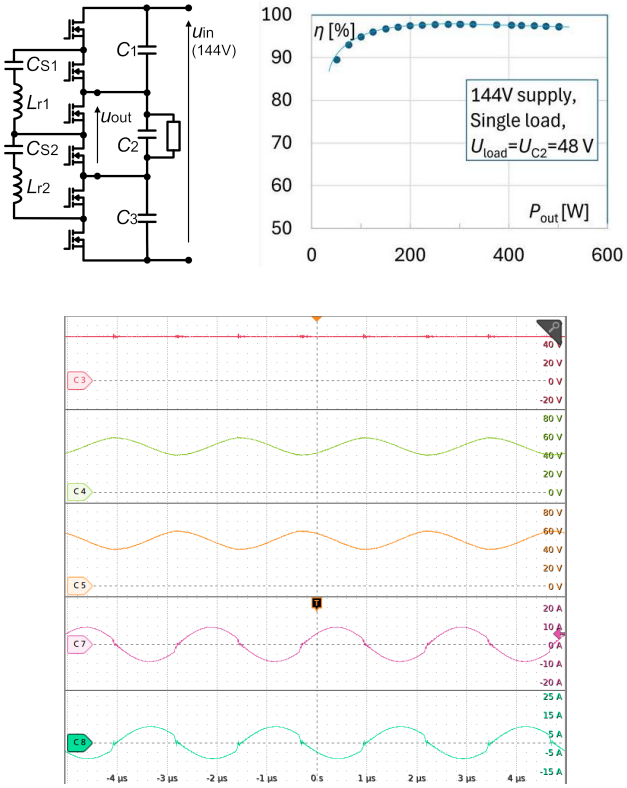


Fig. 26. SC balancer (BC) test circuit configuration, its efficiency and waveforms at P_{out} = 500 W. C3: $u_{C2(load)}$, C4: u_{Cs1}, C5: u_{Cs2}, C7: i_{Lr1}, C8: i_{Lr2}

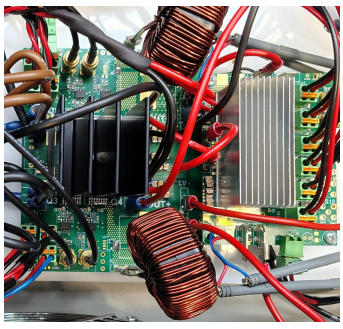


Fig. 27. Experimental setup of HC3L (Fig. 6)

6.2. Hybrid converter HC3L

To demonstrate the operation of the balancing circuit (BC), the case of a hybrid system with three capacitors and maximum asymmetry of load (the load is attached to the middle capacitor as in Fig. 26) was chosen. Figure 27 shows an HC3L laboratory converter (Fig. 6). The switch-mode part uses inductors with an inductance of 150 µH and a much higher volume than those in the SC balancing circuit (BC).

The BC parameters are presented in Table 5. Both parts of the HC3L use GaN transistors. The BC is a low-voltage circuit that allows the use of a small clearance on the PCB. In the demonstrated system, it was made using GaN transistors in a 3×5 mm QFN package with surface mounting and $R_{DS(on)}$ = 1.2 mΩ. A 470 nH resonant inductor is used with dimensions of 12.8×12.8 mm and a height of 6.2 mm, as well as a switched capacitor bank (C_{S1}, C_{S2}) composed of 22 nF, 200 V MLCC capacitors. The switching pattern of a balancing circuit of this type requires the input of one control signal and its inversion on two sections of transistors (Fig. 9). There is no regulation here, and the BC equalizes the voltages on the three capacitors. Figure 26 shows the results demonstrating the operation of such a system, where, through switched capacitors (C_{Sn}), the voltages across the capacitors of the main circuit (C_{1-3}) remain at the same value despite loading only one of them. Operating in ZCS and ZVS modes, such a converter can achieve remarkably high efficiency (97.8% in the test conducted), which is also shown in Fig. 26. Therefore, the BC used is a circuit with low complexity

of topology and control, operating with high efficiency, and configured using low-volume elements.

Table 5
Parameters of the switched-capacitor balancing circuit (BC)

Parameter	Description and value
Conversion voltage	3×48 V
Inductors	L_{rn} = 470 nH (HCI1365-R47)
Transistors	EPC2367 U_{DS} = 100 V, I_D = 101 A, $R_{DS(on)}$ = 1.2 mΩ (typ. value at 25°C)
Switching frequency of a single transistor	f_b = 400 kHz
Dead time	t_d = 20 ns

The measurement results of the hybrid system HC3L (with the balancing circuit BC – Fig. 6) are shown in Figs. 28–32. According to the concept of operation and simulation results, a voltage of 48 V is maintained on the load by the BC working with oscillating overcharges of switched capacitors (Fig. 16). The comparison of the properties of the hybrid converter (HC3L) and the purely switch-mode circuit (SBC – Fig. 1) shows that, in the HC3L, the average values of currents in the inductors of the switch-mode parts are approximately half as high (Fig. 29). This allows the use of inductors with lower inductance in the system with the BC. At 500 W of load power, the power of the BC is approximately 250 W.

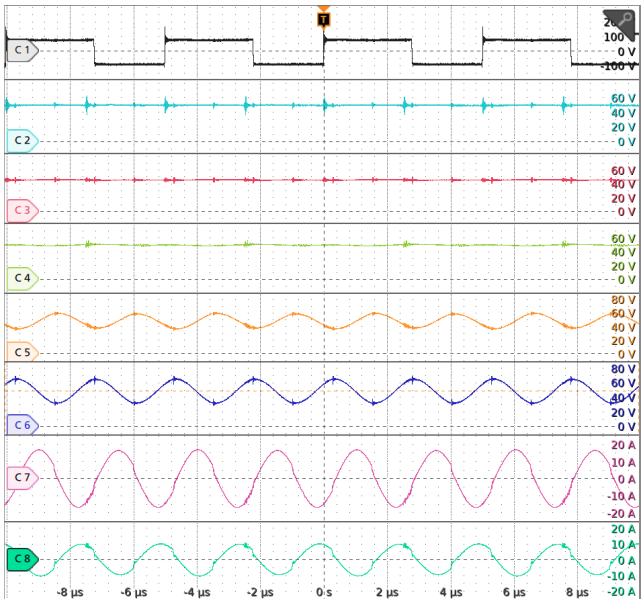
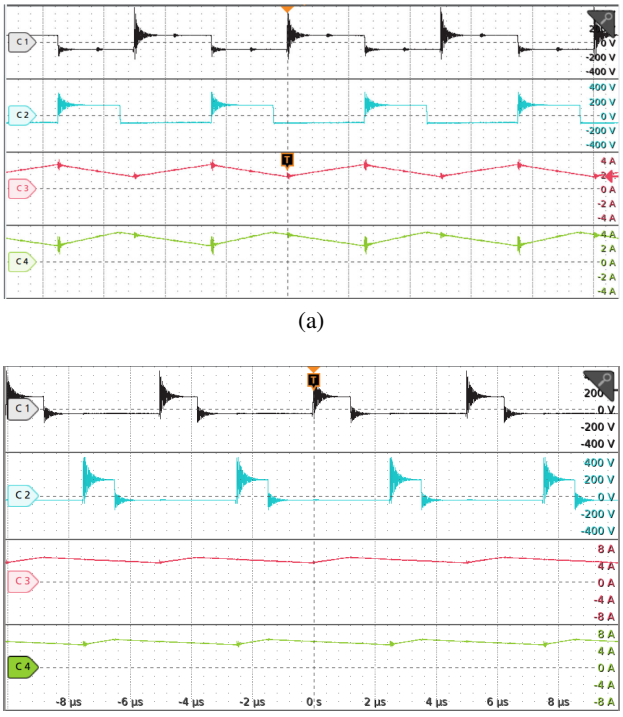


Fig. 28. Experimental results of HC3L (Fig. 6) operating at 400V/48V conversion ratio; $U_{in1} = U_{in2}$, f_S = 200 kHz, f_b = 400 kHz, P_{out2} = 700 W, $P_{out1} = P_{out3}$ = 0 W. C1: u_{L1}, C2: u_{Cout1}, C3: u_{Cout2}, C4: u_{Cout3}, C5: u_{Cs1}, C6: u_{Cs2}, C7: i_{Lr1}, C8: i_{Lr2}

The application of a hybrid system allows for a reduction in the current of the inductors and the use of three outputs. At



(a)

(b)

Fig. 29. Steady-state waveforms at 400V/48V operation, P_{out2} = 500 W (from the top: u_{L1}, u_{L2}, i_{L1}, i_{L2}). (a) HC3L, (b) SBC

the maximum tested load asymmetry of these outputs, where there was only one load, a slight decrease in the efficiency of the converter was observed (Fig. 30). This is due to two factors:

- In the HC3L, the voltage stress of transistor S_3 is greater than that in the SBC, i.e.:

$$P_{oss(SBC)} = \frac{f_S}{2}\frac{1}{8}C_{oss}U_{in}^2 + \frac{f_S}{2}\frac{1}{2}C_{oss}\left(\frac{U_{in}}{2}+U_{out}\right)^2, \quad (19)$$

$$P_{oss(HC3L)} = \frac{f_S}{2}\frac{1}{8}C_{oss}U_{in}^2 + \frac{f_S}{2}\frac{1}{2}C_{oss}\left(\frac{U_{in}}{2}+2U_{out}\right)^2. \quad (20)$$

- In the HC3L, there are energy losses in the balancing circuit BC (Fig. 6, Fig. 26). Assuming zero switching losses and neglecting core losses, the power losses in the BC are the following:

$$P_{BCcond} = \frac{I_{BCm}^2}{2}R_{tot}, \quad (21)$$

where R_{tot} contains R_L, ESR_{Cs}, ESR_{Cout}, and $R_{DS(on)}$ of two transistors in series, and I_{BCm} is the amplitude of current in the BC.

In a switch-mode system with a lower current, the use of inductors with a lower saturation current may allow their volume to be reduced due to a smaller core cross-sectional area. The I^2R resistance losses in the inductor windings are also reduced. Figure 31 shows the results of the thermal measurements of the HC3L. At P_{out2} = 700 W (unbalanced loads $P_{out1} = P_{out3}$ = 0 W), the switch-mode part of the converter and the balancer BC reached a similar temperature with forced airflow. In the

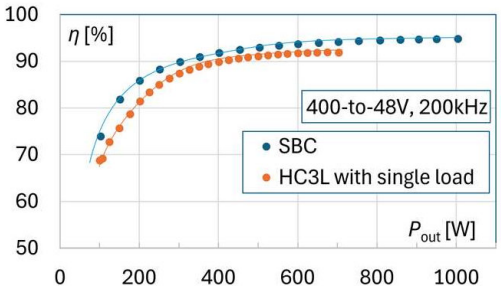


Fig. 30. Experimental efficiency measurement results of HC3L with single load ($P_{out2} < 700$ W, $P_{out1} = P_{out3} = 0$ W) and SBC. Conversion ratio: 400V/48V

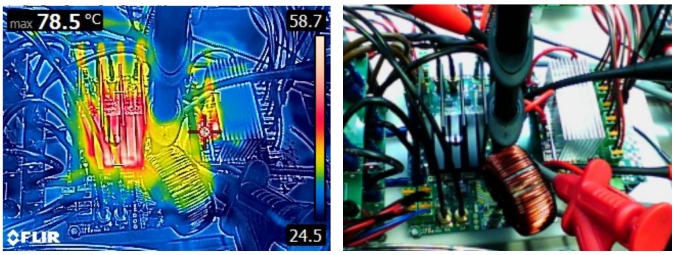


Fig. 31. Thermal results of HC3L (Fig. 6) operating at 400V/48V conversion ratio; $U_{Cin1} = U_{Cin2}$, $f_S = 200$ kHz, $f_b = 400$ kHz, $P_{out2} = 700$ W

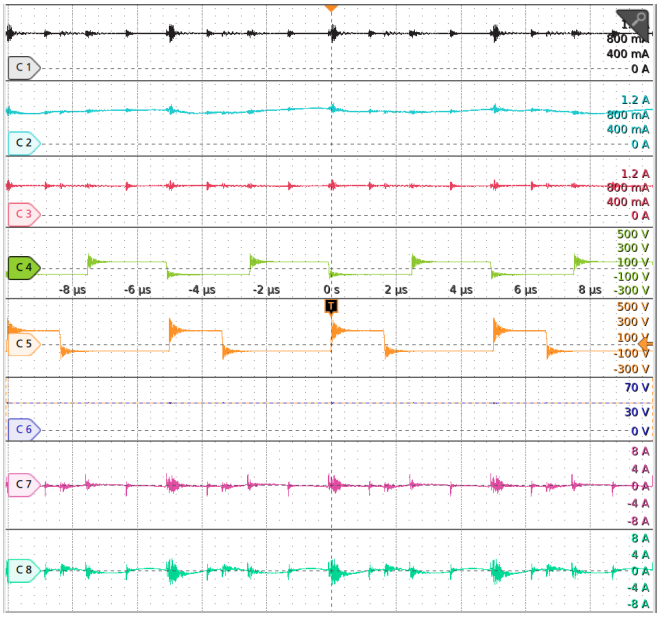


Fig. 32. Experimental results of HC3L (Fig. 6) operating with three loads, at 400V/48V conversion ratio; $U_{in1} = U_{in2}$, $f_S = 200$ kHz, $f_b = 400$ kHz, $P_{out1} = P_{out2} = P_{out3}$: C1: i_{Load1}, C2: i_{Load2}, C3: i_{Load3}, C4: u_{L1}, C5: u_{L2}, C6: u_{Cout}, C7: i_{Lr1}, C8: i_{Lr2}

experimental model presented, this value of the load power was considered to be the maximum when working with maximum asymmetry, $f_S = 200$ kHz, $f_b = 400$ kHz, and the conversion ratio of 400-to-48V. The HC3L can operate with one, two, or three loads (Fig. 6). Figure 32 shows the waveforms in a system with three equal loads. In this case, the load on the output circuit of the balancer BC is less than in a single-load system due to less load asymmetry.

A comparison to the state-of-the-art is presented in Table 6. It includes the most important parameters of the selected convert-

Table 6
Comparison of high step-down converters with gain extension

Ref	Voltage gain	No. of diodes	No. of switches	Efficiency (%)	Gain extension technique	Count of inductors/capacitors	Power rating (W)	In/out voltage (V)	f (kHz)	PIV****
[1]	$D/(2-D)$	2	1	95–96	Switched-inductor hybrid	2 inductors / 2 capacitors	5000	(120–400)/ (50–120)	9	$2U_{in}/(2-D)$
[4]	$D/(4-D)$ $(1-D)$	5	1	86.7	Ćuk-derived SC-SL hybrid	3 inductors / 3 capacitors	1500 (simulation)	380/15	100	$U_{in}/(1-D)$
[5]	0.021	0	7	85–91	4-phase hybrid SC (1 inductor)	1 inductor / 3 flying capacitors	100	$48/(1-2)$	250***** −10000	$U_{in}/2$
[9]	0.17	5	5	~ 85–89	GaN-based high step-down SC-SI converter + soft switching	2 inductors / 5 capacitors	85	48/8	56.5	$U_{in}/2$
[10]	$D/(3-2D)$	4	3	94.4	Step-down n-cell converter	1 inductor / 3 capacitors	170	200V/ (12, 24)	50	$U_{in}(3-D)/$ $(3-2D)$
[17]	$D^2(1-D)^3$	7	3	91–93	Transformerless quadratic-based SC hybrid	5 inductors/6 capacitors	430	600/20	30	$(2+D)/$ $(3-D^2)U_{in}$
Proposed	$D_1 - S_{1,3}$ $D_2/(1-D_2)$ $-S_{2,4}$	0	4*, 8** 10***	94.7* 91.9***	Split switch-mode(*) and SC resonant ladder(**)	2×150 µH* (2×150, 1×1) µH, 1×SC** (2×150, 2×1) µH, 2×SC***	1000*, 700***	400/(48, 72, 120)	200*	$0.62U_{in}$

* switch-mode converter SBC (Fig. 1), ** hybrid converters (Figs. 5a, b), *** hybrid converter HC3L (Fig. 6), **** Peak Inverse Voltage, ***** for simulation results

ers. From this comparison, it is seen that the proposed converter achieves high efficiency at an extremely high pulse frequency. This is an aspect that can be used to optimize the DC-DC converter.

7. CONCLUSIONS

This article presents the concept of a DC-DC high step-down converters with the ability to continuous regulation of the output voltage. The configuration of switch-mode converters in each system enables their connection to an input voltage divider and operation with an input voltage equal to about half the total input voltage. This reduces voltage stress across the transistors in the switch-mode converters.

These systems use two switch-mode converters with phase-shifted control. In such a configuration the inductor current is lower than that of a single-stage buck converter and the converters achieve a larger power range. The results in this paper are demonstrated for a supply voltage of 400 V and an output voltage of 48 V, which is one of the typical battery voltage values. This article also presents the concept of supplying a stack of two or three output capacitors, which allowed one to demonstrate the new properties of such a DC-DC system, which, depending on the configuration, are:

- Ripple cancelation or reduction in the output current
- Further reduction in inductor currents
- Possibility of using one, two, or three loads

Maintaining the rated voltage of the load requires the use of an output balancing device. This is a switched-capacitor-based resonant ladder converter. The balancer operates in ZCS mode. The voltage stress of its transistors is low, equal to the output voltage, i.e., 48 V, and it uses elements with an incredibly low volume. The advantage of the balancing circuit BC is also that it does not require a control system because this type of SC converter ensures functional operation and the use of a control with a constant duty cycle.

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