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Low-noise high-resolution CMOS readout ASIC for silicon strip X-ray detectors

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Abstract

This work presents the design, characterisation, and measurement results of the silicon strip sensor readout circuit for X-ray applications. The key design goals were a noise level below 50 electrons rms, low power consumption (below 10 mW per channel) and a compact layout. The prototype integrated circuit was designed and fabricated in a 180 nm CMOS technology, incorporating eight charge-processing channels, biasing circuits, reset and baseline restoration logic, and a calibration system.

1. Introduction

Performance requirements for X-ray imaging systems used in spectroscopy include high-energy resolution, wide dynamic range, high-count rate capability, and good spatial resolution [1–3]. The use of silicon strip detector technology in X-ray instrumentation has been extensively validated in previous work, particularly in applications requiring high energy and spatial resolution. As demonstrated by Gerndt *et al*. [4], Si-strip sensors offer excellent linearity and low noise characteristics, making them a suitable platform for diffraction-based X-ray analysis. Their modularity and compatibility with multichannel front-end electronics further enable scalable system architectures for large-area imaging and high-throughput spectroscopy. These properties, combined with the maturity of fabrication techniques, position Si-strip solutions as a cost-effective and high-performance choice for a wide range of detection tasks. Achieving a superior energy resolution in X-ray spectroscopy is only feasible if the front-end electronics provides a sufficiently low equivalent noise charge (ENC), while simultaneously allowing for the processing of high input count rates. In multichannel systems, the uniformity of key performance parameters across all read-out channels is essential for the reliable separation of radiation spectral lines. This work presents the design and optimisation of LNSTRIP – a prototype read-out application-specific integrated circuit (ASIC) dedicated to 1D silicon strip detectors with a 75 µm pitch. For noise optimisation purposes, the sensor electrodes were assumed to be 1 cm long with an approximate capacitance of 1.5 pF. The main design objective was to minimise total noise through the careful optimisation of the charge processing chain [5], targeting an ENC below 50 electrons rms without degrading the front-end rate performance [6–8]. To support this, additional digital circuitry was introduced, including a fast reset mechanism for a charge sensitive amplifier (CSA) and a baseline restoration logic. The intended energy range of operation is 4–10 keV, with the nominal input signal corresponding to approximately 2200 electrons, equivalent to the charge generated by an 8 keV photon in silicon.

2. Read-out circuit overview

The prototype front-end ASIC comprises eight identical read-out channels, each integrating a full charge-processing chain: a CSA, a shaping amplifier, and a discriminator. Similar read-out architectures employing charge-sensitive amplifiers and shaping circuits for position-sensitive detection using silicon strip detectors have been previously demonstrated in systems for X-ray applications [9]. The architecture of a single read-out channel is shown in Fig. 1. The CSA core employs a telescopic cascode architecture with a p-channel metal-oxide-semiconductor (PMOS) input

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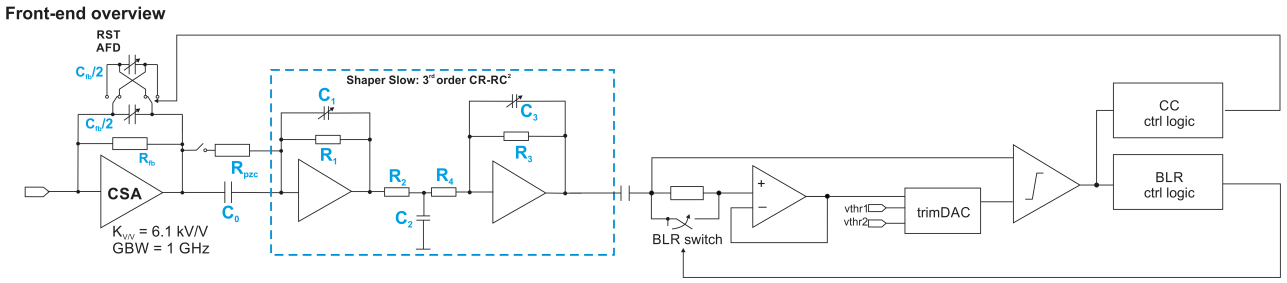

Fig. 1. Charge processing chain overview.

transistor (W/L = 240/0.2 µm), matched to a 1.5 pF detector capacitance. It achieves a gain of 6.1 kV/V and 1 GHz gain-bandwidth (GBW), with a power dissipation under 4 mW per channel.

The feedback network incorporates a 50 fF capacitor, which results in a nominal charge-to-voltage conversion gain of approximately 20 mV/fC. The choice of feedback resistance is critical: it must ensure a sufficiently fast discharge of the CSA following an input event, while simultaneously minimising the contribution of thermal noise to the system performance [7]. In the proposed design, a 10 GΩ MOS resistor operating in the linear region is employed as a feedback element. To further enhance the recovery characteristics of the CSA – particularly in scenarios involving large or closely spaced charge hits – additional digitally-assisted circuits are implemented, providing accelerated discharge support and improved baseline restoration.

The CSA output is connected to a pole-zero cancelation (PZC) circuit that prevents the shaper output baseline shift in the event of a pile-up caused by a long CSA discharge time. The resistance in PZC is also made by the channel conductance of the transistors connected in parallel. The CSA core output is directly connected to the feedback sources and the PZC MOS resistors, at the same potential, with an offset of approximately 100 mV. This ensures the proper operation of the PZC circuit even if the DC voltage level at the CSA output changes [10].

The shaping amplifier is based on a differential folded-cascode operational tranconductance amplifier (OTA) [11] with the reference voltage provided from the pad that makes the performance of this stage adjustable, if necessary. The shaping filter employs a third-order CR-RC² topology, with a default peaking time of 1 µs, adjustable between 0.5 µs and 1.5 µs. The peaking time can be selected using a set of capacitors and resistors together with switches. The shaper parameters were selected to achieve the lowest possible noise in the system [12].

The discriminator stage uses a differential threshold and a 6-bit trimming digital-to-analogue converter (DAC) for bias control, allowing fine-tuning and compensation for process variation.

3. Noise optimisation

Noise in a detector read-out system can be expressed as ENC. The overall noise includes thermal noise, flicker noise, and current noise – see (1):

$$ENC^2 = F_w \frac{1}{\tau_p} C_T^2 a + F_f C_T^2 \frac{A_f}{f} + F_i \tau_p b, \tag{1}$$

where F_w – thermal noise coefficient, a – sum of the core transistors thermal noise, F_f – flicker noise coefficient, A_f – sum of the core transistors flicker noise, F_i – current noise coefficient, b – sum of all current noise components, τ_p – shaping amplifier peaking time, C_T – total input capacitance (of the detector and the input transistor).

Design parameters were selected based on the front-end noise optimisation, ensuring that the total noise is dominated by the CSA input transistor thermal and flicker noise. Contributions from other transistors were minimised via sizing adjustments [13]. Other system components affect mostly the current noise components, expressed as (2):

$$b = 2qI_{\text{det}} + \frac{4kT}{R_f}, \tag{2}$$

where q – elementary charge, I_det – detector leakage current, k – Boltzmann constant, T – temperature, R_f – CSA feedback resistance.

Equation (2) shows that one of the components that form the total output noise in a detector read-out system is connected to the detector leakage current and the CSA feedback resistance. Although the designer has very small or almost no impact on the detector parameters, it is still possible to lower the total ENC by a proper selection of the feedback resistance value. The CSA feedback resistance should be maximised within the constraints of nanometer-scale IC technology. However, this significantly slows down the feedback capacitor discharge process, making the entire system less responsive. Without complete discharge of the CSA feedback capacitor, the incoming charges cause a baseline shift and, as a result, a system saturation. To address the issue discussed above, some features are implemented to speed up charge processing and allow for higher input rates.

4. Read-out modes

Three read-out modes were implemented to support operation across a range of input rates: basic operation with PZC, faster mode with active feedback discharge (AFD), and, additionally, baseline restoration (BLR) circuit.

4.1. Pole-zero cancellation (PZC)

PZC comprises a 10 pF capacitor and a 50 MΩ MOS resistor that cancel the CSA feedback pole, stabilising the baseline during a low-rate operation. Without PZC, voltage drift can reach 30% after prolonged signal activity [10].

4.2. Active feedback discharge (AFD)

To prevent CSA saturation at higher rates, AFD actively resets the feedback capacitor by switching its polarity via control logic triggered by discriminator pulses. This significantly reduces the baseline shift [14]. Upon a signal arrival, the feedback capacitor C_F, composed of two equal parts (0.5 C_F each – one fixed and one switchable), is charged. To efficiently reset the CSA, a control logic block – triggered by the discriminator rising edge – initiates a proper sequence of disconnections and polarity reversals on the switchable part of C_F, effectively discharging the stored charge within a few nanoseconds. This mechanism supports the use of high feedback resistance (to reduce noise), while helping mitigate pile-up effects at the CSA output, as shown in the earlier designs [14].

4.3. Baseline restoration (BLR)

To maintain signal integrity and avoid long-term baseline drift at the shaper output, dedicated baseline holder circuits can be employed [15]. These circuits allow slow correction of the DC level between pulses, while remaining inactive during signal transients. To maintain a stable baseline at the discriminator inputs, and counteract overshoot introduced by AFD, a BLR circuit resets the shaper output voltage level immediately after peaking time. Located at the discriminator input, the BLR is also triggered by the discriminator output [16]. The discriminator pulse is delayed and stretched by a pulse stretcher. The discriminator pulse is delayed and stretched by a pulse stretcher, with the delay time adjustable via a current supplied from a pad.

5. Simulation results

The performance of the circuit was simulated both on the schematic level, as well as extracted post-layout level. The PZC circuit helps maintain the baseline level after incoming input hits as shown in Fig. 2.

Table 1 summarises the performance with and without PZC.

The simulated behavior of the circuit without the active CSA feedback compared to the performance with the AFD switched on is presented in Fig. 3. Comparison of shaping amplifier output before and after BLR presented in Fig. 4 shows that the overshoot caused by the use of CSA reset can be significantly mitigated.

The difference at the discriminator inputs is prone to mismatch and process variations. Therefore, the corner and Monte Carlo (MC) simulations were run. MC simulations were performed using randomised variations of process parameters, including transistor threshold voltages, channel lengths and widths, and temperature-dependent bias conditions, allowing statistical estimation of worst-case ENC

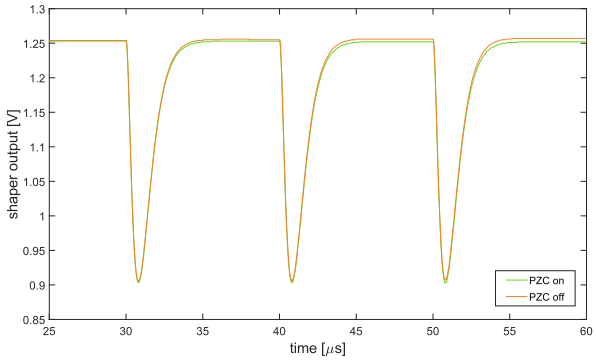

Fig. 2. Shaper output waveforms with (green) and without (orange) the PZC circuit.

Table 1
Performance comparison.

Header	PZC enabled	PZC disabled
ENC (electrons)	22.15	21.91
Noise rms (mV)	4.046	3.998
Shaper output amplitude (mV)	357.0	356.6

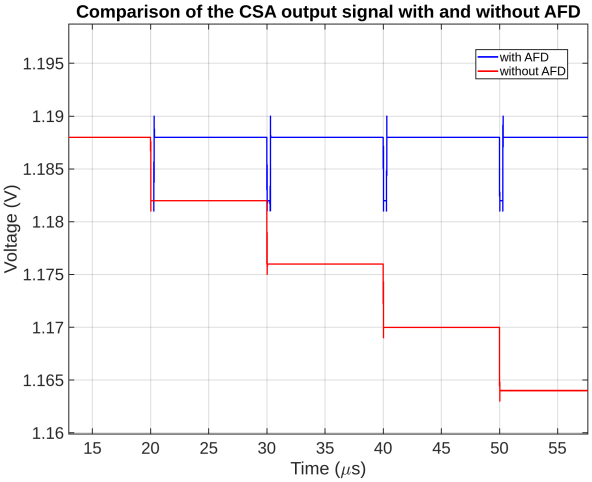

Fig. 3. CSA output waveforms with and without the AFD reset applied.

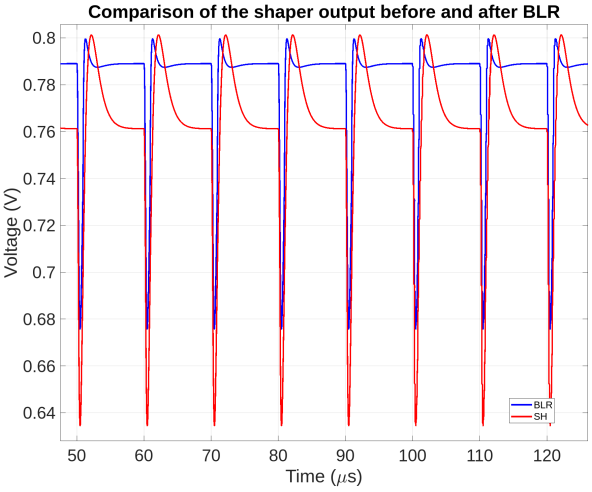

Fig. 4. Shaper output signals before and after the BLR circuit.

values. The selected number of iterations ensures a sufficient confidence interval for estimating input mismatch and trimming DAC effectiveness. The results of the MC (1000 runs) for the discriminator differential input is shown in Fig. 5.

The range of the trimming DACs, marked with a green square in Fig. 5, spans from -280 mV to 280 mV, which is considerably broader than the typical variation of the discriminator input voltage differences. The ENC values from the MC simulations (for 1000 runs), shown in Fig. 6, reach 47 electrons rms for the worst case, which is not very far from the specification. The summary of the MC simulation is shown in Table 2.

The design underwent corner simulations to evaluate its robustness under process, voltage, temperature (PVT) variations. The worst ENC value that can be expected for fast-fast (ff) variation, minimal resistance and capacitance, maximum temperature of 85 °C, is equal to 63 electrons rms. This result suggests that, for operation at very high temperatures, a proper cooling system may be mandatory. The lowest achievable ENC is 16 electrons (slow-slow corner, maximum resistance and capacitance, temperature -10 °C).

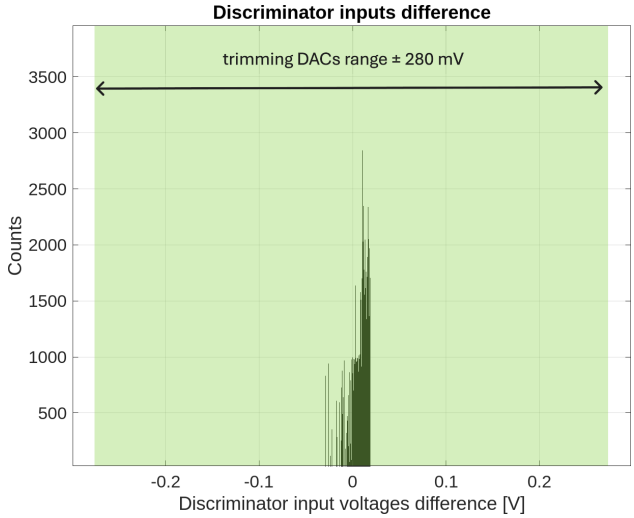

Fig. 5. Differential voltage at discriminator inputs MC simulation (1000 runs).

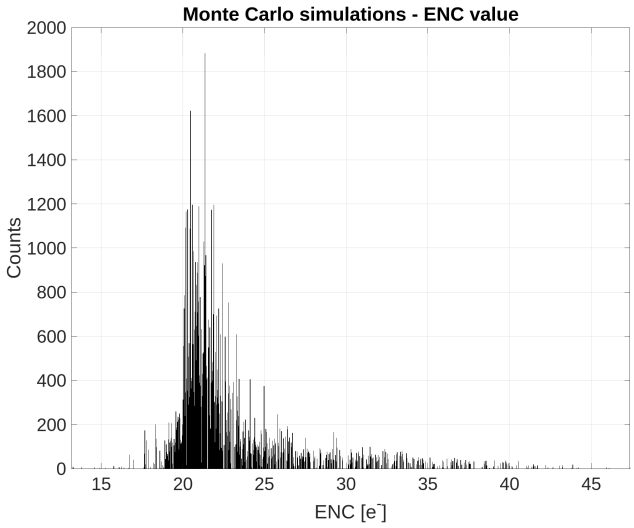

Fig. 6. ENC value – MC simulation (1000 runs).

Table 2
MC simulation summary (1000 runs).

Header	Min. / max.	Mean	Std. dev.
ENC (electrons)	13.18 / 47.38	24.87	6.14
Noise rms (mV)	1.62 / 7.60	4.23	1.05
Shaper output amplitude (mV)	181.70 / 366.50	334.70	24.20
CSA output amplitude (mV)	6.0 / 7.4	7.20	0.27

6. Design implementation

The design was implemented in a 180 nm complementary metal-oxide-semiconductor (CMOS) process on a die of 1.5 µm × 3.2 µm area. Although the 180 nm CMOS technology node is no longer considered cutting-edge in terms of digital density, it offers several compelling advantages for mixed-signal and radiation-tolerant applications. Its relatively large feature size ensures better analogue performance, higher supply voltage headroom, and greater resilience to total ionizing dose (TID) effects, which are critical for robust operation in harsh environments such as space, high-energy physics experiments, or medical systems involving high-intensity radiation sources. Apart from charge processing channels, it also contains biasing circuits and DACs, and a small area is occupied by another digital design from a separate project – see Fig. 7. Post-layout simulations demonstrated that the layout of the CSA reset circuitry is critical to its proper operation and should be carefully optimised to minimise coupling between the AFD control lines and the CSA input/output signal lines. To eliminate the CSA baseline jumps, significant modifications were made to the control line layout. After compensation, the baseline jumps do not exceed 0.3 mV, which corresponds to approximately 5% of the CSA output amplitude for the default input charge value (2200 electrons).

The design was submitted for fabrication in Q3 2024 and is now ready for measurements – the ASIC photo is presented in Fig. 8. Currently, the test setup is being designed, including the test printed circuit board (PCB) dedicated to wire-bonding of the ASIC. The PCB will be equipped with all necessary biasing circuits and connectors. Signal integrity tests will be performed using a mixed-signal oscilloscope and a programmable pulse generator. In addition to basic functional tests, noise measurements under varying temperature and biasing conditions will be conducted to confirm the simulation results. The presented IC comprises an internal calibration circuit that allows for test charge injection and basic characterisation of the read-out channels. The tests with a semiconductor detector are also planned.

7. Conclusions

This work presents the design and characterisation of a low-noise, high-resolution CMOS read-out ASIC tailored for 1D silicon strip X-ray detectors. The LNSTRIP prototype successfully meets the stringent requirements of modern X-ray

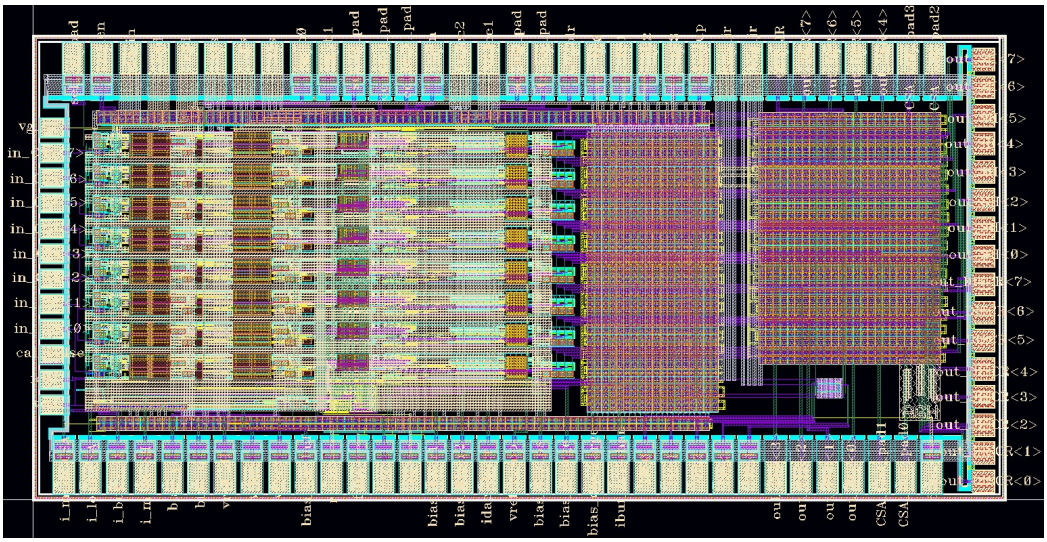

Fig. 7. The layout of the LNSTRIP ASIC.

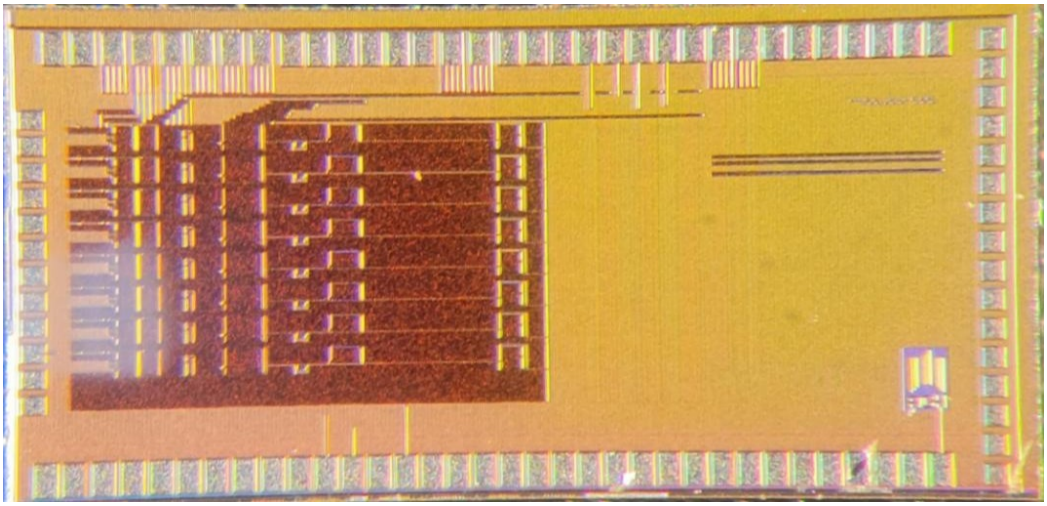

Fig. 8. The fabricated LNSTRIP ASIC real photo.

spectroscopy, offering an ENC below 50 electrons rms, low power consumption under 10 mW per channel, and support for high input rates through integrated fast reset and BLR circuits. Simulation results, including MC and PVT corner analyses, demonstrate robust performance and minimal parameter variability in process variations. The fabricated ASIC, implemented in the 180 nm CMOS technology, is currently undergoing test preparations with further evaluation planned using real detector systems. The developed solution offers a compact and efficient front-end read-out architecture, paving the way for its integration into high-performance spectroscopic and imaging systems. Future development of the presented architecture will focus on extending the number of read-out channels and integrating on-chip analogue-to-digital conversion. Additionally, efforts will be directed toward implementing real-time digital signal processing for hit detection and energy discrimination, which would enable standalone operation without requiring external back-end electronics. Testing in irradiation and temperature-variable environments is also planned to assess the long-term robustness of the ASIC.

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