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Comparative analysis of a noise and count-rate performance of a charge-sensitive amplifier in planar CMOS and FinFET technologies for hybrid pixel detectors

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Abstract

This paper presents a comparative analysis of a charge-sensitive amplifier (CSA) for hybrid pixel detectors operating in a single-photon counting mode, implemented in a 40 nm planar complementary metal-oxide-semiconductor (CMOS) and a 16 nm fin field-effect transistor (FinFET) technologies. Hybrid pixel detectors are widely used in particle physics, synchrotron radiation facilities, and X-ray imaging applications, where front-end electronics must support increasingly high photon flux while maintaining low noise and a compact pixel area. A folded-cascode charge-sensitive amplifier was designed in both technologies and evaluated through circuit simulations in terms of open-loop gain, gain-bandwidth product, maximum counting rate, and equivalent noise charge (ENC). The 16 nm FinFET implementation achieved significantly higher intrinsic gain and gain-bandwidth product than the 40 nm planar CMOS design, resulting in a substantially higher maximum counting rate while maintaining comparable noise. These performance improvements, however, come at the cost of increased design complexity, reduced flexibility in transistor sizing, greater sensitivity to layout parasitics, and higher fabrication costs. The results demonstrate that FinFET technology offers strong potential for next-generation high-speed front-end readout electronics for hybrid pixel detectors, particularly in applications requiring high count-rate capability, while highlighting the design trade-offs associated with advanced technology nodes.

1. Introduction

Recent advances in CMOS technology have significantly expanded the capabilities of analogue and mixed-signal integrated circuits. In particular, the transition from conventional planar CMOS processes to deeply scaled multi-gate technologies, such as FinFETs, has enabled higher operating speeds, lower power consumption, and increased integration density [1]. These improvements are particularly advantageous for hybrid pixel detectors (HPDs) operating in single-photon counting (SPC) mode, where stringent requirements for timing performance, electronic noise, power dissipation, and pixel size must be simultaneously satisfied.

Initially developed for high-energy physics experiments, HPDs have become an established detection technology in numerous scientific, industrial, and medical applications [2] due to their excellent spatial resolution, high count-rate capability, and near-noiseless photon detection [3]. In particular, synchrotron radiation facilities increasingly rely on photon-counting HPDs for X-ray diffraction [4], scattering [5], and imaging experiments in materials science, structural biology, and pharmaceutical research [6–9]. The next generation of diffraction-limited storage rings is expected to provide X-ray beam intensities up to two orders of magnitude higher than those available at current facilities, imposing increasingly demanding requirements on detector front-end electronics and readout architectures. Many X-ray scattering and diffraction techniques require high angular resolution to accurately reconstruct structural information from diffraction patterns [10]. This can be achieved by increasing the distance between the sample and the detector or by employing detectors with smaller pixel pitches. Consequently, there is a growing demand for hybrid pixel detectors offering both higher intrinsic spatial resolution and the capability to operate under substantially increased photon fluxes. Current state-of-the-art photon-counting HPDs typically feature pixel pitches ranging from 50 μm to 100 μm [11]. These detectors

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provide direct digital image acquisition with excellent noise performance and support virtually dead-time-free operation, enabling duty cycles approaching 100%.

Despite these advantages, the maximum achievable count rate of photon-counting detectors remains fundamentally limited by pulse pile-up in the in-pixel analogue front-end and counting circuitry [12]. At high photon fluxes, overlapping pulses result in counting losses and nonlinear detector response, restricting the practical count-rate capability of existing systems to a few million photons per second per pixel. Overcoming this limitation while simultaneously reducing pixel dimensions represents one of the major challenges in the development of next-generation hybrid pixel detectors for high-brilliance synchrotron sources, particularly for coherent scattering techniques that require both high photon throughput and enhanced spatial resolution.

To address the challenges associated with the development of next-generation HPDs, advanced circuit architectures and fabrication technologies must be investigated. Accordingly, this work focuses on the design and comparative evaluation of a charge-sensitive amplifier (CSA), which constitutes a key component of the analogue pixel readout front-end electronics. The CSA is implemented in two contemporary CMOS technology nodes: a 40 nm planar CMOS process and a 16 nm FinFET-based CMOS technology. Although FinFET devices have become the dominant solution for digital integrated circuits, their suitability for low-noise analogue front-end electronics remains an active area of research [13–16].

Preliminary research on a CSA implemented in FinFET technology was presented during a conference [15], demonstrating the potential of advanced technology nodes to achieve higher count rates. The present work extends that research by providing a detailed analysis of the factors responsible for the performance differences between the two CSA implementations. In particular, it investigates pile-up handling in SPC systems, noise minimisation, and CSA speed optimisation. Following a brief introduction to the architecture of HPDs in section 2, section 3 provides a comparative overview of planar CMOS and FinFET technologies. Section 4 describes the CSA design at the schematic level. Section 5 compares the key parameters of the input transistors used in the two technologies. Finally, section 6 presents the simulation results for the CSAs designed in 40 nm and 16 nm technologies and analyzes their impact on the overall CSA performance, with particular emphasis on noise and maximum count rate.

2. Hybrid pixel detector architecture

A HPD consists of two independently optimised components: a pixelated semiconductor sensor and a readout integrated circuit (ROIC), interconnected by bump-bonding technology, as shown in Fig. 1. The ROIC comprises a two-dimensional array of pixel front-end circuits responsible for signal amplification, discrimination, and photon counting.

2.1. Sensor material

The design of ROIC for an SPC operation depends on the properties of the sensor material and the intended X-ray energy range. Key design considerations include X-ray absorption efficiency, leakage current, charge collection time, and charge-sharing effects. The semiconductor materials most commonly used in HPDs are Si [17], Ge [18], GaAs [19], CdTe [20], and CdZnTe [21].

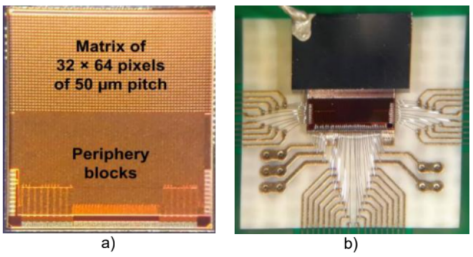


Fig. 1. Example prototype of a hybrid pixel detector developed at AGH University [12] for the extremely brilliant source (EBS) upgrade of the European Synchrotron Radiation Facility (ESRF): (a) ROIC and (b) sensor bump-bond to ROIC.

One of the main advantages of the hybrid detector architecture is the ability to combine the same ROIC with different sensor materials. Silicon is widely used because of its excellent charge transport properties and low leakage current; however, its X-ray absorption efficiency decreases significantly above approximately 20 keV. As many next-generation synchrotron facilities are designed to operate at higher X-ray energies and increased photon fluxes, high-Z semiconductor materials such as CdTe and CdZnTe have become attractive alternatives, because of their superior absorption efficiency.

2.2. Signal processing chain in SPC mode

In an SPC mode, each charge pulse generated by the sensor is processed independently by the corresponding pixel front-end. A typical pixel circuit consists of a CSA, a discriminator (DISCR), and a digital counter (COUNT), as shown in Fig. 2. The CSA integrates the charge generated by an absorbed photon and converts it into a voltage pulse. This pulse is then compared with a programmable threshold by the discriminator and, if the threshold is exceeded, the corresponding counter is incremented by one. Threshold discrimination effectively suppresses electronic noise and dark current fluctuations, enabling direct digital image acquisition with a high signal-to-noise ratio and excellent spatial resolution.

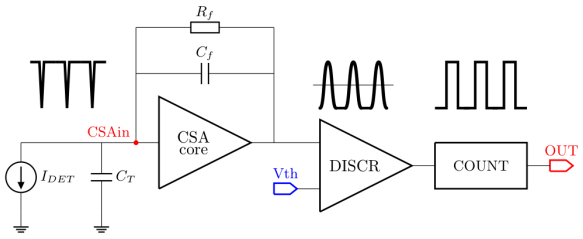


Fig. 2. Simplified schematic of the pixel front-end electronics operating in SPC mode.

Following photon absorption, the CSA integrates the generated charge in the feedback capacitor C_f. Assuming a sufficiently high open-loop voltage gain K_0 of the amplifier such that $K_0 C_f \gg C_T$, where C_T is the total input

capacitance, including the sensor capacitance C_{SEN}, the input transistor capacitance and parasitic interconnect capacitances, the output voltage amplitude can be approximated as:

$$V_{OUT,max} = \frac{Q_{IN}K_0}{(K_0+1)C_f + C_T} \approx \frac{Q_{IN}}{C_f}. \quad (1)$$

As shown in (1), the charge-to-voltage conversion gain is primarily determined by the feedback capacitance. Therefore, a small feedback capacitance together with a low total input capacitance is desirable to maximise the output signal amplitude. Another key performance parameter of SPC pixel circuits is the maximum sustainable count rate, which is mainly limited by pulse pile-up. This effect occurs when two or more photon-induced pulses overlap in time at the CSA output, leading to counting errors and degradation of detector linearity (see Fig. 3) .

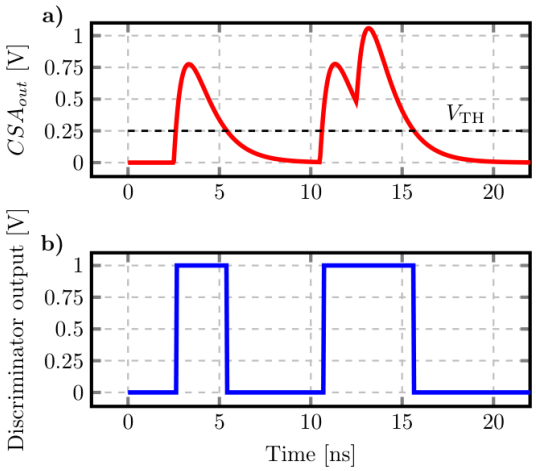


Fig. 3. Representative waveforms demonstrating the pile-up effect (a) CSA output, (b) discriminator output.

The CSA output pulse is described by [2]:

$$V_{OUT}(t) = \frac{Q_{IN}}{C_f}\frac{\tau_f}{\tau_f - \tau_r}(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}}), \quad (2)$$

where the fall and rise time constants are given by:

$$\tau_f = R_f C_f \quad (3)$$

and

$$\tau_r = GBW\frac{C_T}{C_f}, \quad (4)$$

respectively, where R_f is the feedback resistance, and GBW is the gain bandwidth product of a CSA. In such a circuit, the maximum pulse amplitude is determined by the relationship [2]:

$$V_{OUT,max} = \frac{Q_{IN}}{C_f}\beta, \quad (5)$$

where

$$\beta = \left(\frac{\tau_f}{\tau_r}\right)^{\frac{\tau_r}{\tau_r - \tau_f}}. \quad (6)$$

The most straightforward approach to mitigate pulse pile-up is to reduce the CSA output pulse width. According to (2), the pulse width is primarily determined by the fall-time constant τ_f and can be reduced by decreasing the feedback resistance R_f or the feedback capacitance C_f. However, reducing R_f or C_f introduces a trade-off between pulse duration, signal amplitude, and circuit stability [22]. As the rise- and fall-time constants become comparable, the peak output amplitude decreases, as described by (5). Therefore, shortening the CSA output pulse also requires reducing the rise-time constant τ_r, which can be achieved by increasing the GBW of the core amplifier (4). The resulting reduction in peak signal amplitude leads to a further degradation of the equivalent noise charge (ENC), as discussed below. The dominant source of noise in a CSA is typically the input transistor. Its power spectral density (PSD), which comprises both thermal and flicker noise components, can be expressed as [2]:

$$\frac{\overline{V_{nw}^2}}{df} = \frac{4\gamma kT}{g_m} + \frac{K_f}{C_{ox}WL}\frac{1}{f}. \quad (7)$$

where k is the Boltzmann constant, g_m is the transconductance of the input transistor, T is the absolute temperature, K_f is the flicker noise coefficient, C_{ox} is the gate oxide capacitance per unit area, W is the transistor channel width, L is the transistor channel length, f is the frequency and γ takes the value $\frac{1}{2}$ in weak inversion and $\frac{2}{3}$ in strong inversion. For fast signal shaping at the CSA output, the thermal noise generated by the feedback resistor should also be taken into account. Its power spectral density (PSD) is given by [2]:

$$\frac{\overline{i_R^2}}{df} = \frac{4kT}{R_f}. \quad (8)$$

The sensor itself contributes to the overall noise through its leakage current, I_{leak}, which generates shot noise. Moreover, the sensor capacitance plays an important role in determining the ENC, as discussed later. The corresponding shot-noise PSD is given by:

$$\frac{\overline{i_{leak}^2}}{df} = 2qI_{leak}, \quad (9)$$

where q is the elementary charge. Using the procedure described in [2], the noise voltage is calculated at the circuit output. This noise voltage is usually related to the input by dividing the output signal $\frac{q\beta}{C_f}$ of a single electron, see (5). The resulting parameter is the ENC [23, 24].

$$ENC_{total}^2 = \frac{1}{(q\beta)^2}\left(\frac{kT\gamma C_T C_f}{C_L} + kTC_f + \frac{qI_{leak}}{2}R_f C_f + \sqrt{\frac{K_f}{C_{ox}WL}}\sqrt{\ln(GBW\tau_f C_f C_T)}\right), \quad (10)$$

where C_L is the capacitance at the high-impedance output node of the CSA core. In (10), β quantifies the effect of the relative separation between the rise and fall time constants on the signal amplitude at the CSA output, as described by (6). Maintaining β close to unity is therefore essential for minimising ENC at high count rate.

The previous equations indicate [(2)–(6)] that obtaining a fast CSA circuit with a short output pulse requires reducing the fall time constant τ_f. Similarly, to avoid degrading circuit noise performance, the parameter β must remain close to unity. Reducing the feedback capacitance C_f decreases both the noise contributions of the circuit (10) and the fall time constant (3). However, this causes the time constants

τ_f and τ_r to converge, which in turn worsens β (6) and therefore increases the ENC (10). An alternative approach to improve the count rate of the circuit is to adjust the feedback resistance R_f which decreases τ_f without directly altering τ_r. A third approach to decoupling the time constants while simultaneously increasing the signal amplitude is to increase the transconductance g_m of the input transistor. This results in a higher gain-bandwidth product (GBW) and a shorter rise time τ_r, as given by (4). However, this improvement usually comes at the cost of increased power consumption. These observations show that a trade-off between power, speed, and noise is inevitable in circuit design. Table 1 summarises several counting circuits implemented in sub-micrometer CMOS technologies and lists their parameters that satisfy the aforementioned trade-off.

3. Comparison of planar FET and FinFET CMOS technologies

Contemporary demand in the semiconductor industry is driven primarily by digital applications, such as processors, graphics accelerators, and memory chips. Consequently, most technological development effort has been directed towards parameters relevant to digital circuit design. Although FinFET technology emerged as a natural continuation of planar CMOS scaling and was originally motivated by these digital requirements, several of its structural features turned out to be advantageous for analogue circuit design as well. In a conventional planar transistor [(Fig. 4(a)], the source, drain, and channel are formed within the plane of the substrate, with a single gate positioned above the channel to modulate current flow. FinFET devices depart from this arrangement by raising the channel above the substrate surface into a thin, vertical structure – hence the name, drawing an analogy to a fin breaking through the water surface [(Fig. 4(b)]. Wrapping the gate around this elevated channel provides substantially tighter electrostatic control over channel formation, and arranging multiple fins closely together allows a considerable reduction in the transistor footprint. However, these benefits are offset by greater complexity in both fabrication and circuit design.

The improved gate control characteristics of FinFET devices is reflected in a higher on-state current I_{ON}, due to increased transconductance g_m, together with a reduced off-state leakage I_{OFF} [14]. According to [1], this tighter electrostatic control also suppresses the drain-induced barrier lowering (DIBL), which in turn increases the output resistance of the device and, consequently, its intrinsic gain. On the other hand, FinFET technology is not free of drawbacks: parasitic capacitances and resistances tend to be larger [30], and phenomena such as electromigration (EM) and self-heating (SHE) [31]. Furthermore, the noise characteristics of FinFET devices differ from those of conventional planar MOSFETs, with both thermal and flicker noise requiring careful consideration in low-noise analogue applications [32].

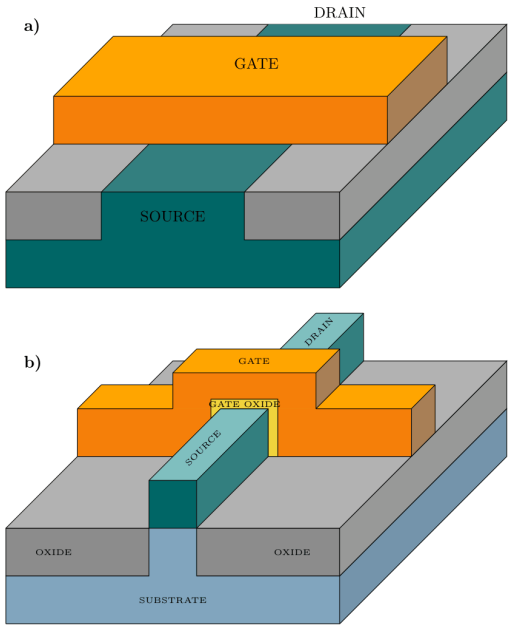


Fig. 4. Illustrative MOS transistor structures in planar CMOS and FinFET technologies.

4. CSA core design

For the purpose of this comparison, a CSA core amplifier was implemented separately using 40 nm planar CMOS

Table 1
Comparison of counting circuits in sub-micron CMOS technologies.

Chip [ref]	Medipix 3RX [25] [23]	PXD18k [26]	Eiger [27] [23]	UFCX32k [28]	IBEX [29] [23]	SPHIRD-1 [12]
Process	130 nm	180 nm	250 nm	130 nm	110 nm	40 nm
Pixel size [μm^2]	55×55	100×100	75×75	75×75	75×75	50×50
Power/pix.* [μW]	9	23	–	26	8	17.6
ENC [el. rms]	80	168	175	235	90	188
10% dead time loss input rate per pixel# [Mcps]	0.26	0.61	0.82	1.23	1.11	4.4

* Static PWR consumption
# Calculated using minimum dead time and assuming $N_{OUT}/N_{IN} = 0.9$ according to the formula $N_{OUT} = N_{IN} \exp(-N_{IN}\tau_p)$ where N_{OUT} and N_{IN} are the output and input pulse value, respectively .

transistors and 16 nm FinFET devices, with the feedback network – comprising the resistor and capacitor – represented at this stage by ideal RC elements. Even at the schematic level, the two technologies impose noticeably different design constraints. Older, planar CMOS nodes offer a relatively straightforward transistor structure, which in turn permits a wide range of channel dimensions to be freely selected. This flexibility is particularly valuable in circuit blocks that combine transistors of markedly different sizes. Figure 5(a) shows the folded-cascode CSA core implemented using this approach. The 40 nm technology enables transistor M0 to be designed with a wide gate and a short channel length, maximising its transconductance. In contrast, transistor M1, which operates as a current source, benefits from a longer channel length to improve current source performance. FinFET technology, by contrast, substantially limits the designer's freedom in selecting transistor width and length. Channel length can still be varied to some extent, typically among a small set of predefined values, but doing so is constrained by strict layout rules: transistors sharing a common channel length must be placed on a fixed grid, and mixing different lengths within the same block requires additional spacing to satisfy design rule check (DRC) requirements. The resulting longer interconnects introduce higher parasitic capacitance and resistance. A practical way around this limitation is to keep a single channel length throughout the entire block and, wherever a longer effective channel is needed, achieve it by stacking multiple transistors of the same type in series – an approach referred to in the literature as the "Poor Man's Cascode" [33]. This technique was adopted for the CSA core implemented in 16 nm FinFET, shown in Fig. 5(b).

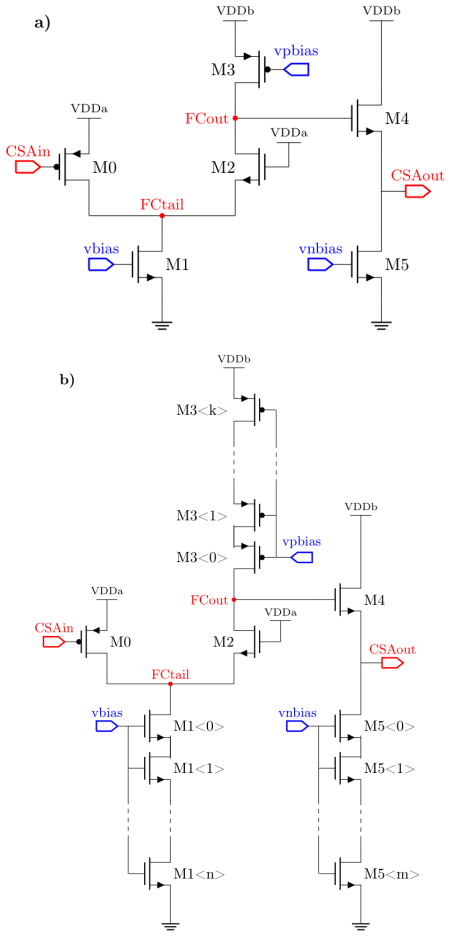


Fig. 5. CSA core schematic (a) in 40 nm planar CMOS technology; (b) in 16 nm FinFET technology.

5. Transistor parameters in the selected nanometers CMOS technologies

The choice of fabrication technology has a direct impact on transistor-level performance. This section reports the parameters obtained for the CSA input transistor in both the 16 nm FinFET and 40 nm planar CMOS processes.

Figure 6(a) confirms that, for the transistor sizing adopted here, the 16 nm FinFET device reaches a considerably higher intrinsic gain than its planar counterpart, which in turn improves the overall amplification provided by the CSA core; a higher core gain reduces the sensitivity of the output amplitude to the input capacitance C_T. A comparable trend is observed for g_m/I_D [Fig. 6(b)]: at a matched drain current, the FinFET transistor delivers a larger transconductance, which is expected to yield higher gain, a faster rising edge (4) and lower noise (10).

The remaining parameters, listed in Table 2 for a fixed drain current of $I_D = 5$ µA, further confirm that the FinFET input transistor combines higher transconductance with a higher output resistance (lower g_{ds}), in agreement with previously reported observations [13].

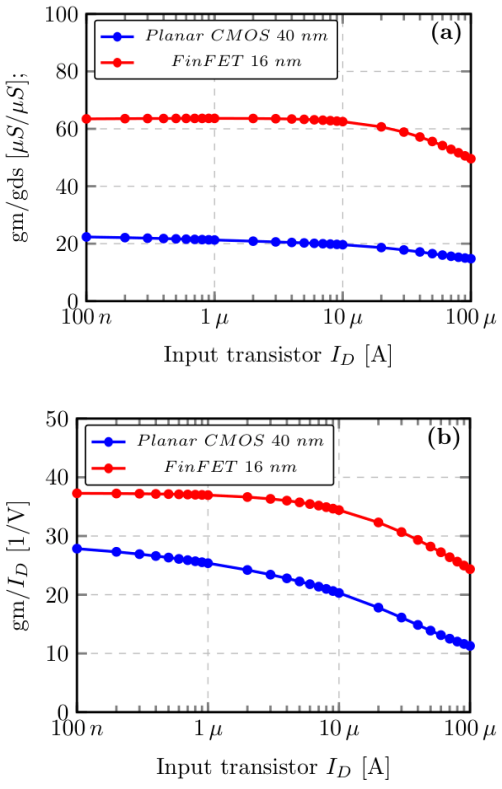


Fig. 6. Input transistor parameters (a) intrinsic gain $\frac{g_m}{g_{ds}}$; (b) $\frac{g_m}{I_D}$.

Table 2
Comparison of CSA core parameters.

Parameter	Unit	Planar 40 nm	FinFET 16 nm
$\frac{W}{L}$	$[\frac{\mu m}{\mu m}]$	$40 \times 0.16/0.080$	$12 \times 0.25/0.036$
I_D	[μA]	5	5
$\frac{g_m}{g_{ds}}$	$[\frac{\mu S}{\mu S}]$	20.3	62.1
g_m	[μS]	108.9	167.3
g_{ds}	[μS]	5.4	2.7
$\frac{g_m}{I_D}$	$[\frac{\mu S}{\mu A}]$	22.2	33.8
C_{GD}	[fF]	3.4	2.0
C_{DD}	[fF]	0.8	0.8
C_{SS}	[fF]	2.4	1.4

However, a notable caveat concerns parasitic capacitance. Although schematic simulations indicate values similar to those of the planar process, post-layout extraction typically shows a marked increase in these parasitics, which degrades the achievable circuit bandwidth [13].

6. Simulation results

Subsequently, the two CSA implementations were compared at the circuit level, using a sensor capacitance of C_{SEN} = 50 fF, a feedback capacitance of C_f = 2.4 fF, and a feedback resistance ranging from 0.7 MΩ to 3 MΩ. In both cases the input transistor was biased at 5 μA.

Consistent with the transistor-level results, the 16 nm implementation exhibits a considerably higher open-loop gain than the 40 nm design (K_0 = 60.3 dB *vs.* 44.4 dB), at the cost of a somewhat reduced bandwidth (Fig. 7). The net effect is a larger gain-bandwidth product, reaching 5.7 GHz in 16 nm compared with 2.8 GHz in 40 nm, in accordance with

$$GBW = K_0 \times BW, \tag{11}$$

where K_0 is converted to linear scale and BW denotes the 3 dB bandwidth of the amplifier.

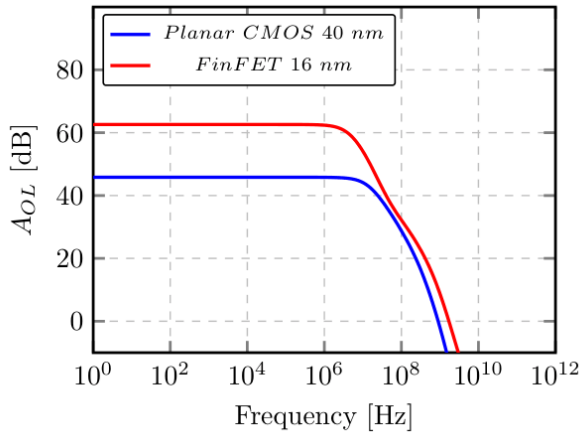


Fig. 7. Gain *vs.* frequency of the CSA core amplifier in 16 nm and 40 nm CMOS technologies.

The higher GBW of the 16 nm CSA core reduces the rise-time constant, as described by (4). This advantage is evident in Fig. 8, which compares the simulated CSA output waveforms for the 16 nm and 40 nm implementations for R_f ranging from 0.7 to 3 MΩ. Reducing R_f accelerates the discharge of the feedback capacitor C_f, thus shortening the output pulse. However, a lower R_f also reduces the peak output amplitude, as predicted by (5) and (6), and can compromise stability.

The effect of the technology-dependent GBW is particularly evident for R_f = 0.7 MΩ. While the 16 nm CSA remains stable, the 40 nm implementation exhibits pronounced oscillatory behaviour due to the lower GBW of its core amplifier. The 16 nm CSA therefore achieves a shorter pulse while maintaining the required stability and limiting the undershoot to the target level of 5%. In the 40 nm implementation, stable operation requires $R_f \geq 1$ MΩ, which suppresses the oscillation but increases the pulse duration (see Fig. 8).

The counting-rate performance of each design was then assessed by applying input pulses with Poisson-distributed arrival times. As a consequence of the lower feedback resistance and the lower rise time constant, the 16 nm design supports a substantially higher counting rate (Fig. 9). At the point where the output rate drops by 10% relative to the input rate, the 40 nm and 16 nm implementations reach 20 Mcps and 32 Mcps, respectively; allowing for a 30% loss however, increases these figures to 70 Mcps and 106 Mcps.

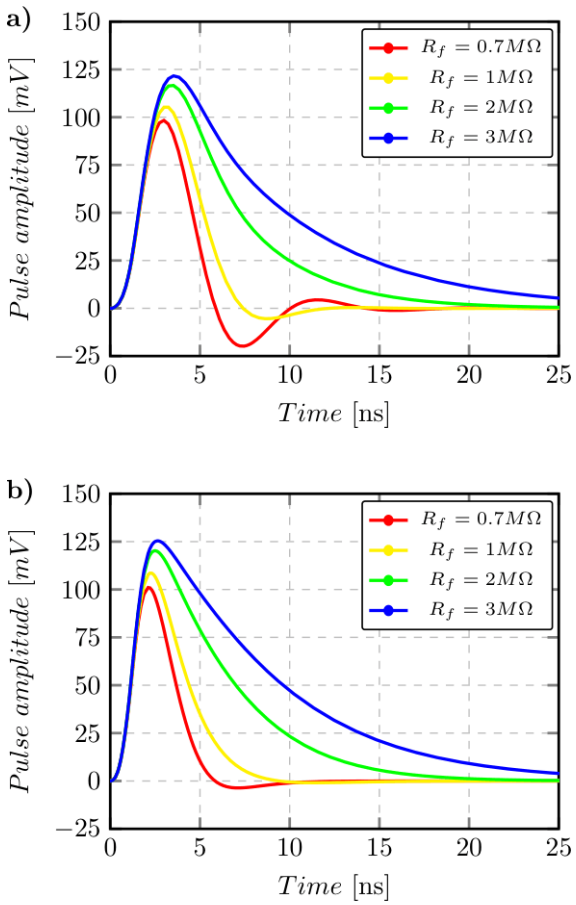


Fig. 8. CSA output pulses for various R_f values for the following technologies: (a) 40 nm planar CMOS, (b) 16 nm FinFET.

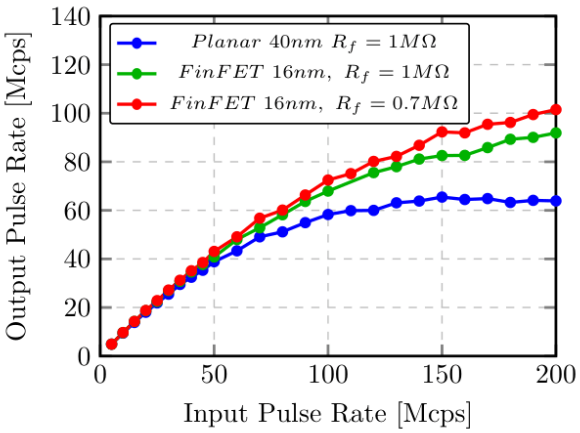


Fig. 9. Count rate performance for CSA with R_f = 1 MΩ in 40 nm technology and CSA with R_f = 0.7 MΩ and R_f = 1 MΩ in 16 nm technology.

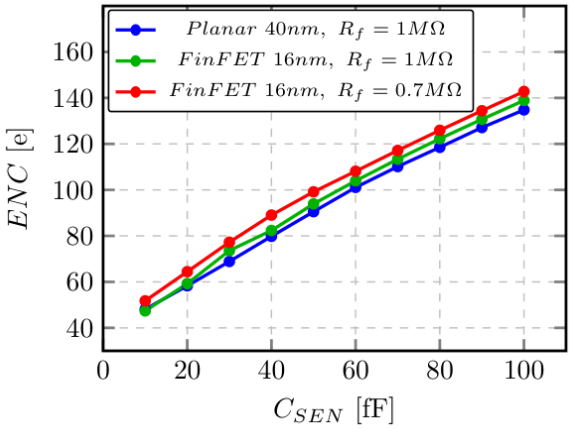


Fig. 11. ENC as a function of the sensor parasitic capacitance for CSA with R_f = 1 MΩ in 40 nm technology and CSA with R_f = 0.7 MΩ and R_f = 1 MΩ in 16 nm technology.

To compare the noise performance of the two technologies, we first consider the same feedback resistance, R_f = 1 MΩ, for both implementations. Individual noise contributions, summed in quadrature, are shown in the pie charts in Fig. 10. The resulting ENC is 92 el. rms for the 40 nm implementation and 94 el. rms for the 16 nm implementation, indicating comparable noise performance. In both technologies, the dominant noise contributions originate from the thermal noise of the input transistor M_0 and current-source transistor M_1. The $\frac{1}{f}$ noise contribution of M_0 is negligible, accounting for only 4% of the total noise power in 16 nm technology. For the 16 nm implementation, further reducing R_f to 0.7 MΩ increases the ENC to 99 el. rms primarily due to the reduced CSA output pulse amplitude.

As predicted by (10), the ENC strongly depends on the total input capacitance C_T, which is dominated by the sensor capacitance C_{sen}. This dependence is shown in Fig. 11 for the CSA configuration considered in the text.

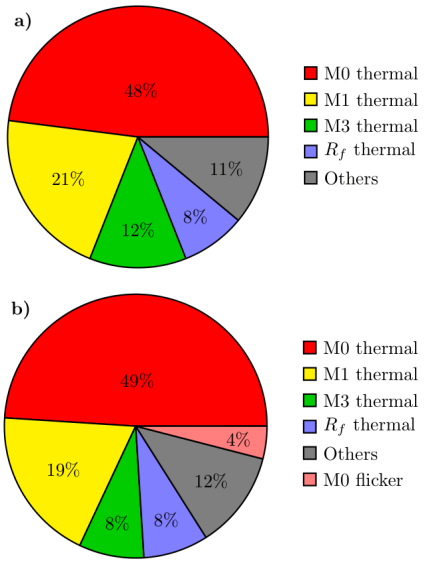


Fig. 10. Percentage breakdown of noise power in CSA for the following technologies: (a) 40 nm planar CMOS, (b) 16 nm FinFET.

7. Conclusions

This work has compared two folded-cascode CSA implementations realised in 40 nm planar CMOS and 16 nm FinFET technologies. The FinFET design was found to offer a markedly higher intrinsic transistor gain and a higher g_m/I_D ratio, which together enable a substantially faster counting rate without a significant penalty in noise performance. However, these gains come with several trade-offs: greater design complexity, stronger dependence of circuit performance on layout parasitics, and reduced freedom in choosing individual transistor dimensions. Taken together, the results suggest that FinFET technology represents a promising route towards faster and more power-efficient front-end readout electronics for future hybrid pixel detector systems.

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Declaration on the use of AI

During the preparation of this manuscript, the authors used an LLM for language editing and grammatical refinement. All scientific content, results, and conclusions are authors' own; the authors reviewed and edited the text after using the tool and take full responsibility for the content of the publication.

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